BACKEND IMPLICATIONS FOR THERMAL EFFECTS IN 3D INTEGRATED SOI STRUCTURES

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Introduction

- Considerable interest in increasing on die device density by using wafer level 3D integration.
- One aspect of the new technologies that has to be addressed is the thermal impact of the backend technology.
- Some of the issues that need to be investigated are:
  - Joule heating in the backend (electrical resistance increases with T – nonlinear).
  - Low-k materials (Thermal conductivity scales with k).
  - Heat flow through the interconnect (complex geometry).
  - Use of thermal vias and design rules to minimize temperature rises. (Optimization)

Modeling approaches

- A number of approaches to the analysis of this heating in electrical devices have been taken including analytical and numerical models.
- The problem is quite complex with a need to solve both the device heating on the surface of the wafer and the line heating in the backend itself.
- The physics involved in solving for the conductive heat flow in a VLSI structure requires solving the following partial differential equation:

$$\rho C \frac{dT}{dt} = \nabla(\kappa(T)\nabla T) + g_{dev}(x,y,z,t) + g_{line}(x,y,z,t,T) = 0 \tag{1}$$

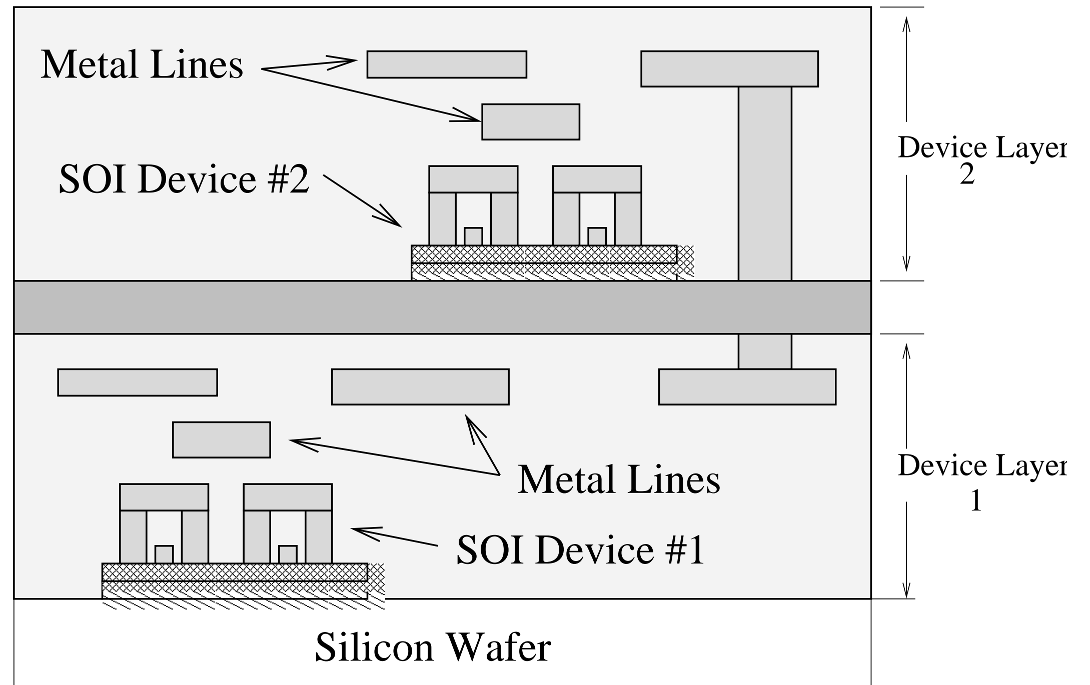
with $\rho = \rho_0 + \alpha T$ and $g_{line}(T) = j^2 \cdot (\rho_0 + \alpha T)$

Atar – A thermal simulator

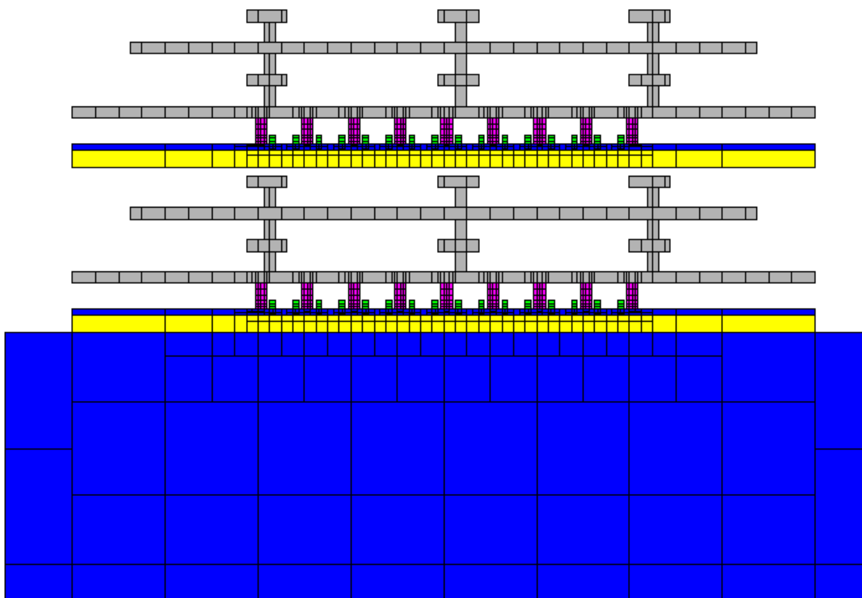
- Our solution to this problem is a simulator that given a technology description and layout information will automatically generate a 3D model of the device, discretize the model, and solve for the temperature distribution in the device.
- *Atar* is thermal simulation tool that uses a technology description and layout information to automatically generate a full 3D model, complete with discretization, and then solves for the temperature distribution.
- Very flexible non-uniform, multi-model meshing allowing for meshes spanning the deep-submicron to the package.
- Produces a self-consistent solution incorporating the temperature dependance of the ohmic heating in the lines.

3D Silicon on Insulator Technology

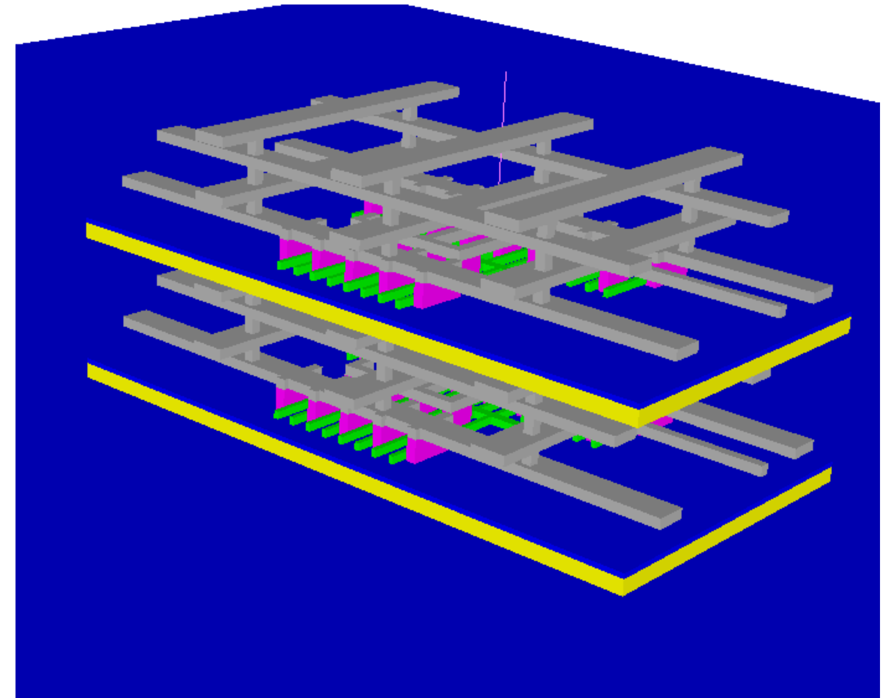
- 3D integration scheme
- bonding of SOI based devices directly on top of the backend of SOI devices.
- The bonding layer used in this scenario is a thin dielectric layer
  (0.3 μm thick).



Atar Model of 2 layer device



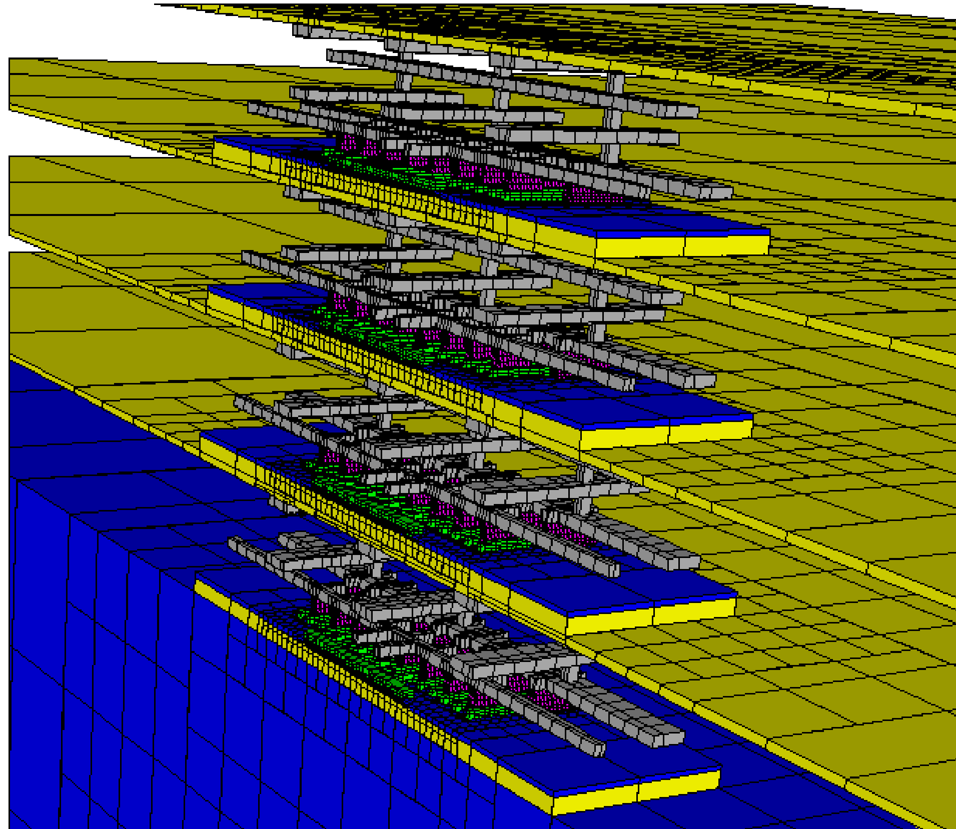
Side View



Perspective View

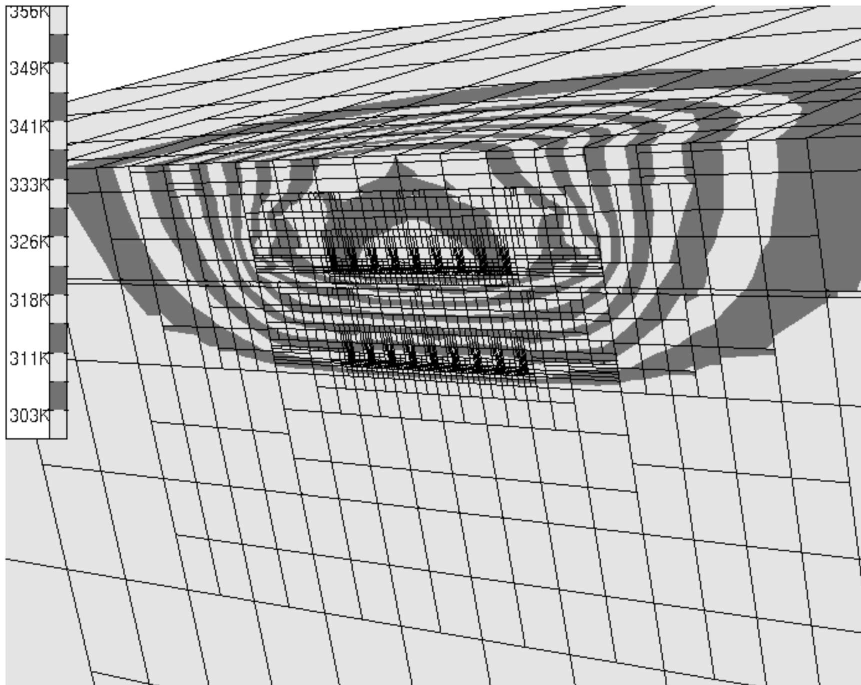
Side and perspective view of *Atar* model with SiO_2 filling material being removed.

Atar Model of 4 layer device



Perspective view of four layer structure with bonding layers shown.

Results: Typical Contour Plots



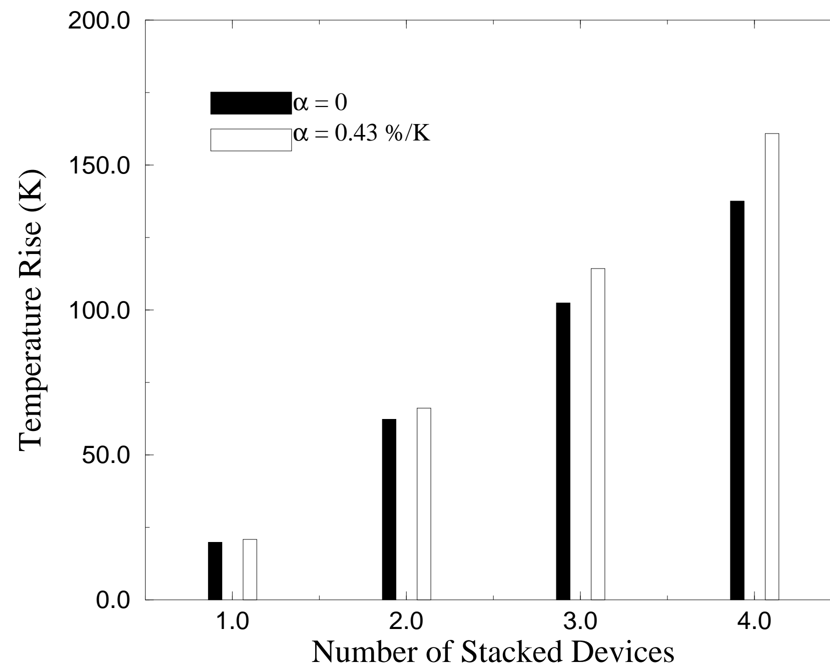
Side View

View of top Device Island

Temperature contours simulated with *Atar* for two layer device.

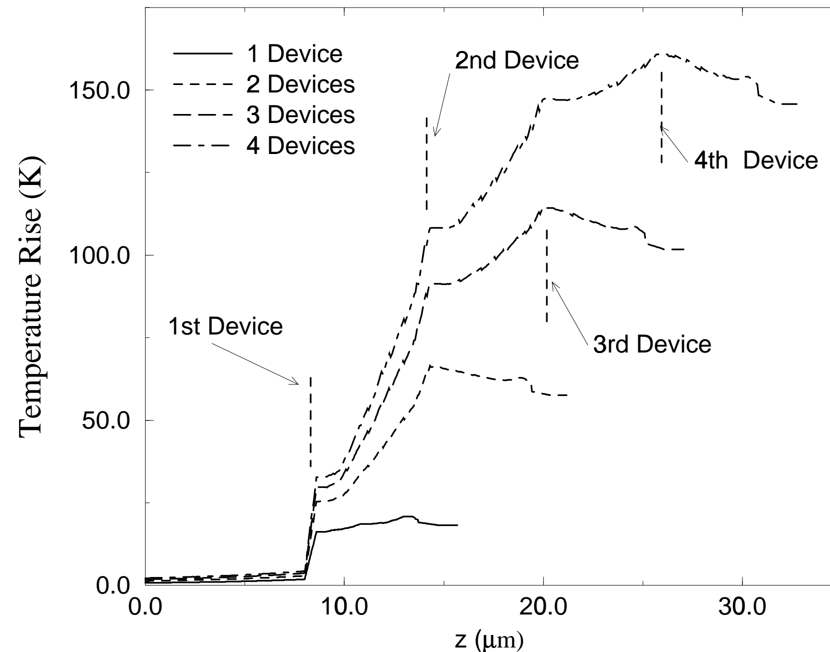
Results: Joule heating in the backend

- Volumetric heat dissipation in the metal were assigned varying from 0.0136 to 0.0444 mW/μm^3 corresponding to M1 through to M4.
- TCR value of Copper
- Temperature increase due to the effect of $\rho = f(T)$ is in the range of 6% for a structure with two stacked devices



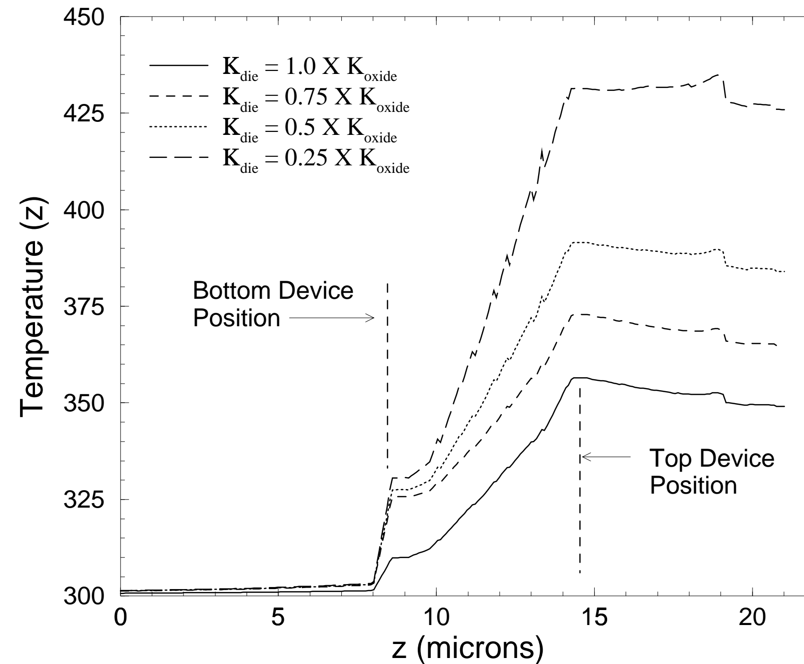
Results: Temperature as Function of the Number of Device Layers

- Plot of the nodal temperatures in the vertical z-direction from 10 μm below the silicon to the top of the backend
- Four models with 1-4 Device Layers
- Three and four level devices are becoming quite hot (unacceptable?)



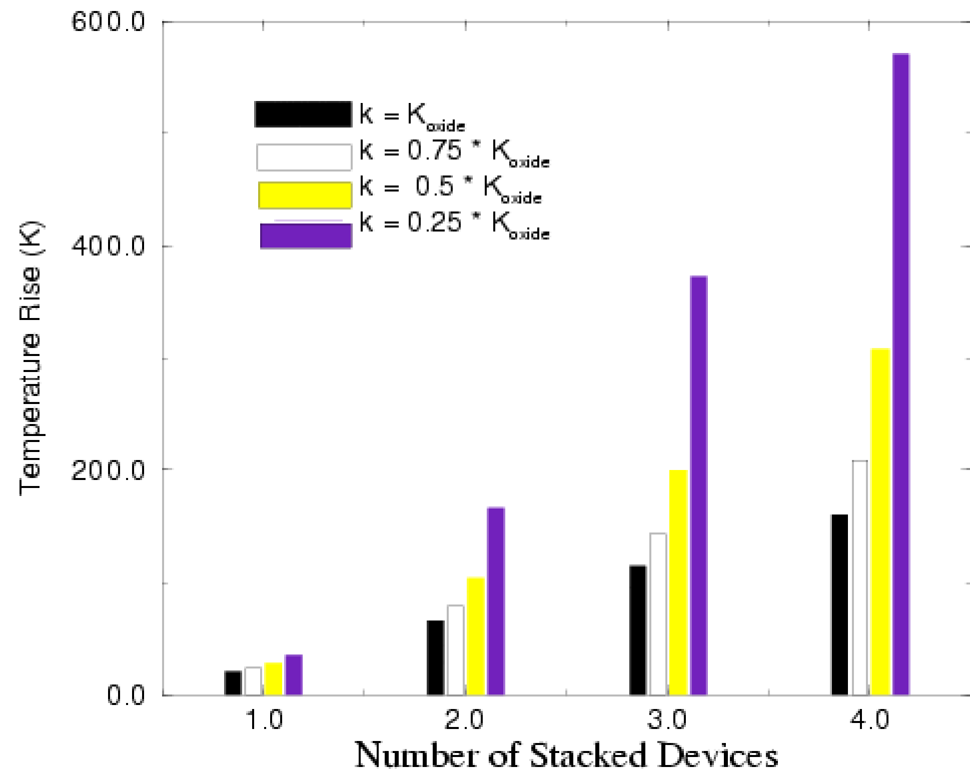
Results:The Effect of low-k Materials

- Much lower thermal conductivity then SiO_2
- Two device layer structure plotted in z-direction variety of thermal conductivities.
- Dramatic increase in temperature rise.



Results:The Effect of low-k Materials

- Much worse for one to four stacked devices
- 75K rises are occurring with a 25% reduction in the thermal conductivity of the back-end material for even two layer device
- Three and four level structues above 200K rises

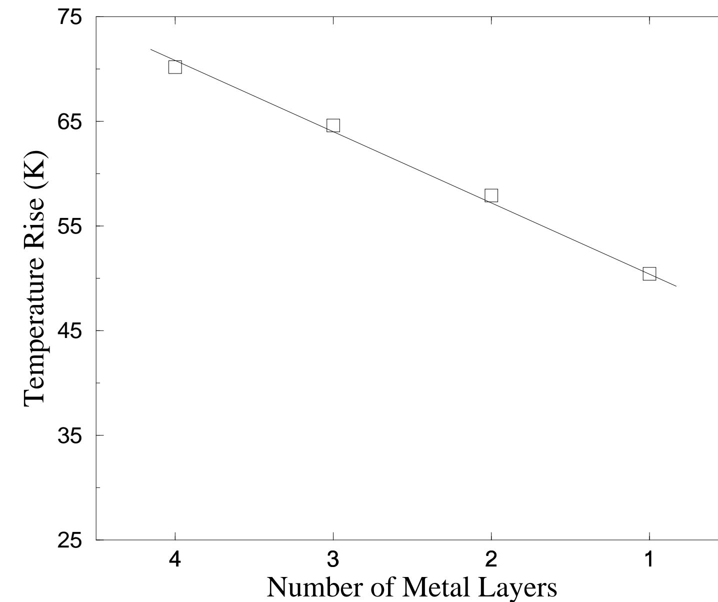


Results: Device Layout and Backend Structure

- The examples before were worst case simulations (stacked high powered devices)
- Possible solutions to lower these temperature rises?
  - Reduce the number of local layers of interconnect from 4 to 3-1 and decrease thermal resistance to Si substrate.
  - Use design rules to disallow stacking and forcing a minimum offset between devices.
  - Use of metal lines as heat spreaders and thermal vias.

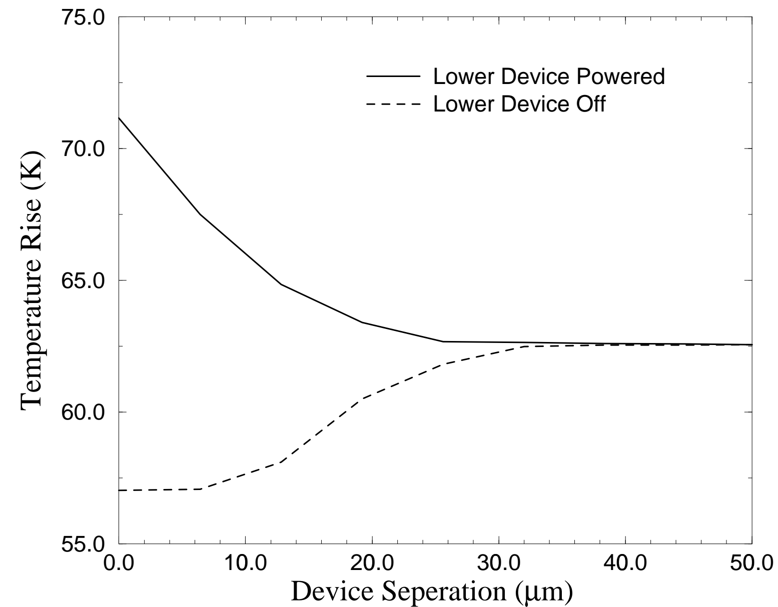
Results: Removing Local Interconnect Layers

- Two device layer structure
- Linear variation as local interconnect layers were removed.
- Almost a 50% reduction in temperature of top device.



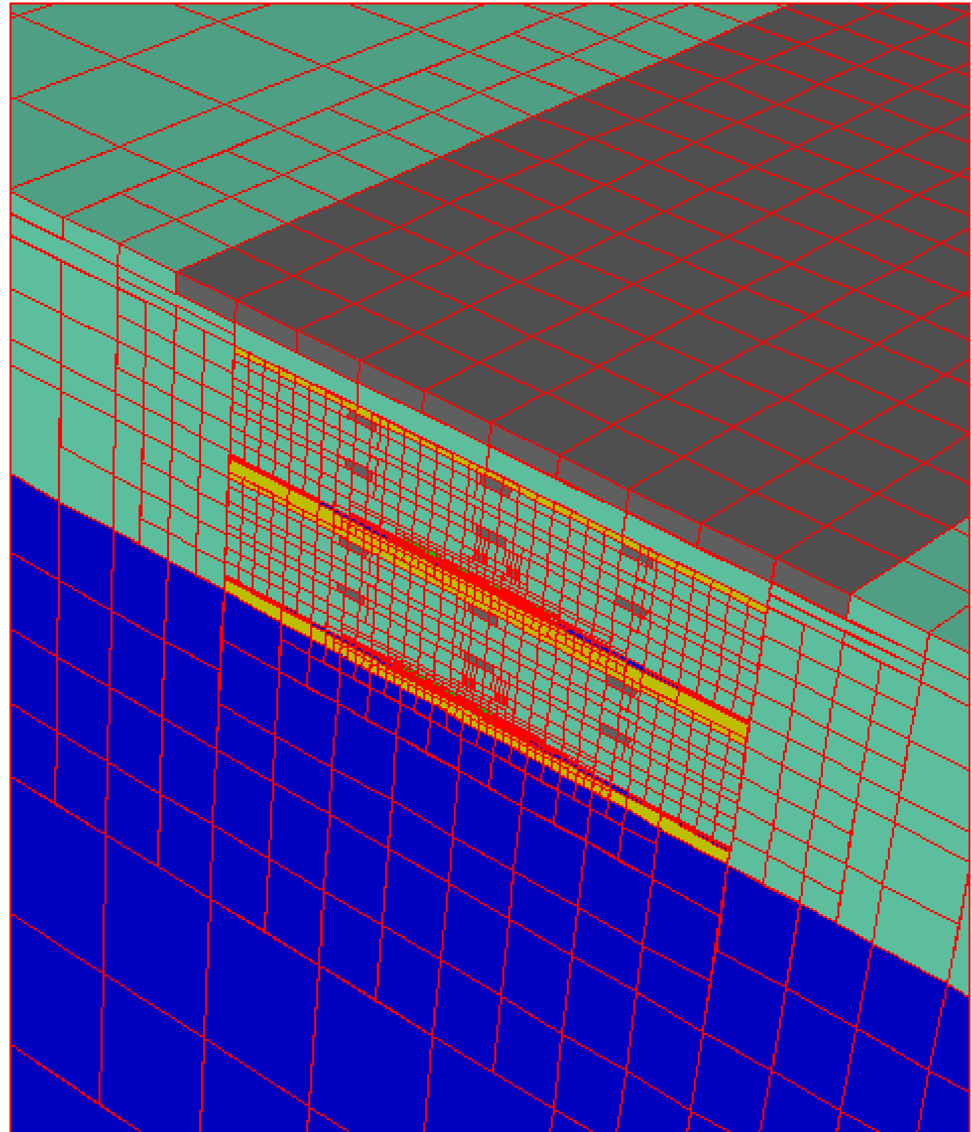
Results: Off-setting The Top device

- Two device layer structure
- Two cases 1) bottom device powered; 2) bottom device off.
- Substantial drop in temperature is obtained if the device is off-set by 20 μm or more
- Cooling effect at zero offset due the the local interconnect for case 2 (lower device off).



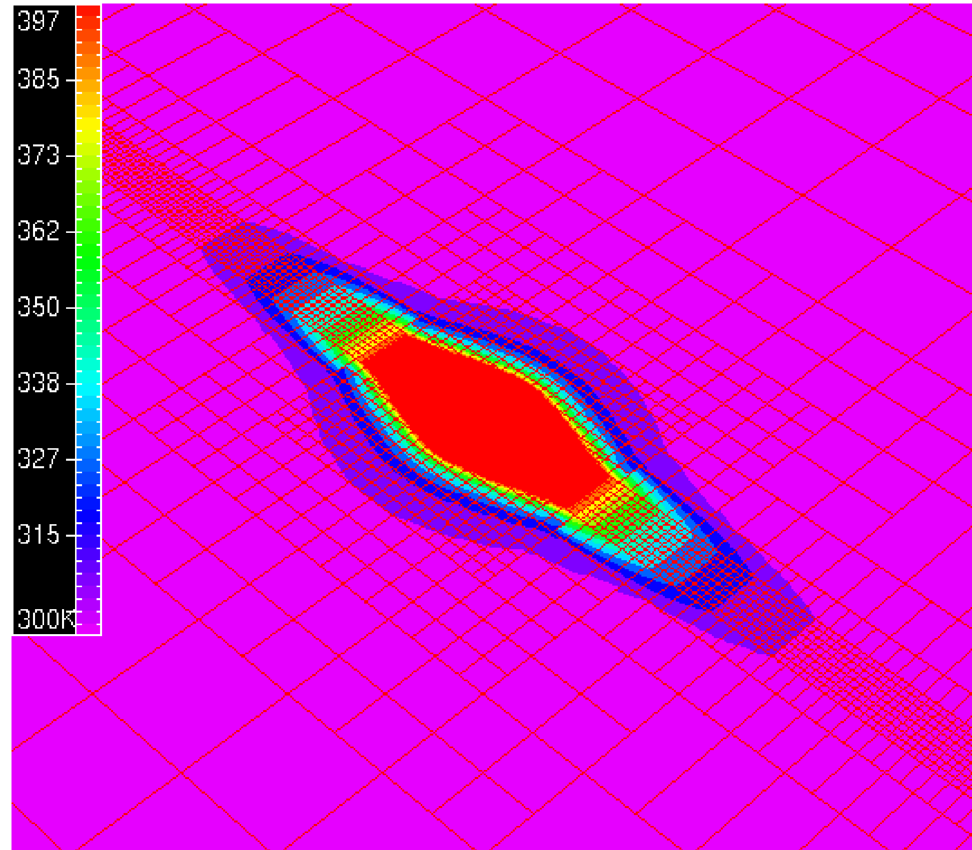
Results: Effect of Nearby line

- *Atar* model built with upper layer metal line present.
- Two cases powered and un-powered bottom device.
- This line can have one of two effects on the simulation.
  - Heat Spreader (line un-powered)
  - Heater (line powered)



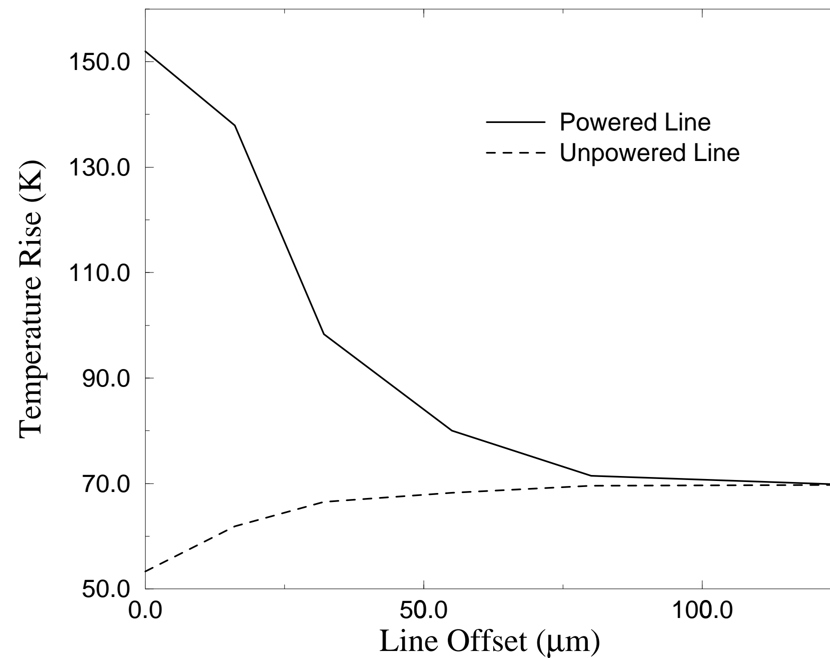
Results: Device Layout and Backend Structure

- Contour plot depicting heat spreading for un-powered line.
- Significant raising of the device temperature by powered line.



Results: Device Layout and Backend Structure

- Offset of 100 μm is need to reduce the heating effect to negligible level.
- Cooling effect less significant.



Conclusions

- Simulation results clearly indicate the importance of the thermal effects in 3D integration structure.
- The inclusion of Joule heating in the backend is found to be important.
- detailed thermal analysis will have to be performed in early design stages including choice of materials.
- Layout issues and design rules will need to be analysed.