Name: ______________________________

Student Number: _________

CARLETON UNIVERSITY

FINAL EXAMINATION April 2016

DURATION: 3 **HOURS** **Number of Students: 46**

Department Name & Course Number: ELEC 4609 Section A

Course Instructors: N.G. Tarr

Authorized Memoranda: Non-programmable calculators **NO BOOKS OR NOTES**

Students **MUST** count the number of pages in this examination question paper **before** beginning to write, and report any discrepancy immediately to a proctor. This question paper has nine (9) pages.

This examination question paper **may not** be taken from the examination room.

In addition to this question paper, students require:	an examination booklet	yes ~	no ~
	a Scantron sheet	yes ~	no ~

ANSWER ALL QUESTIONS

ALL ANSWERS MUST BE WRITTEN ON THE EXAM PAPER
(If necessary, continue answers on the back of pages)

SEE LAST TWO PAGES OF EXAM FOR DATA AND FORMULAS

WRITE YOUR NAME OR INITIALS ON EACH PAGE

Question	Mark
1	
2	
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5	
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Total	

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1. Fig. 1.1 on p. 7 shows the layout of a circuit fabricated in an n-well CMOS technology similar to that used in Lab 2. The layout is not complete: the p+ mask is not shown. Draw the outline of this region (or regions) on the layout, and indicate the interior of the region(s). (*Note*: In this CMOS technology, by default any region that is not covered by the p+ layer receives the n+ implant) *4 marks*

2. In the space provided next to the layout in Fig. 1.1, carefully sketch a cross-section through the integrated circuit along line X-Y (i.e., show how the IC would look if cut along line X-Y and viewed from the side). Indicate the n-well and n+ and p+ regions on your cross-section. *16 marks*

3. a) Underneath the layout of Fig. 1.1, draw the circuit schematic corresponding to the layout. Show the substrate (body) connection for each transistor. *12 marks*

   b) Determine the *W*/*L* ratio for each transistor and write it on the circuit schematic. *2 marks*

   c) On the circuit schematic, circle the transistors that are subject to the body effect. *2 marks*

   d) Complete the truth table in Fig. 1.2 on p. 7. What logic function does this circuit perform? *10 marks*

   e) Suppose input A is held low while input B is switched from low to high. Have the transistor sizes been chosen correctly so that V_{OUT} is at midrail when B is at midrail ($V_{DD}/2$)? Explain. *4 marks*

4. A student now in third year is planning to take ELEC4609 next year. They ask you for advice on how to complete the IC design project to produce a working design with as little effort as possible. On the basis of your experience, what advice would you give them? *5 marks*

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5. Fig. 5.1 shows the schematic for a sense amplifier for a DRAM. The LATCH signal instructs the amplifier to sense the voltage difference between the left and right bit lines. Transistor M3 has $L = 2\ \mu\text{m}$ and $W = 6\ \mu\text{m}$. The gate oxide thickness $t_{ox} = 25$ nm. $V_{Tn} = -V_{Tp} = 0.5$ V and $\mu_n = 2\mu_p = 600\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$. $V_{DD} = 3$ V.

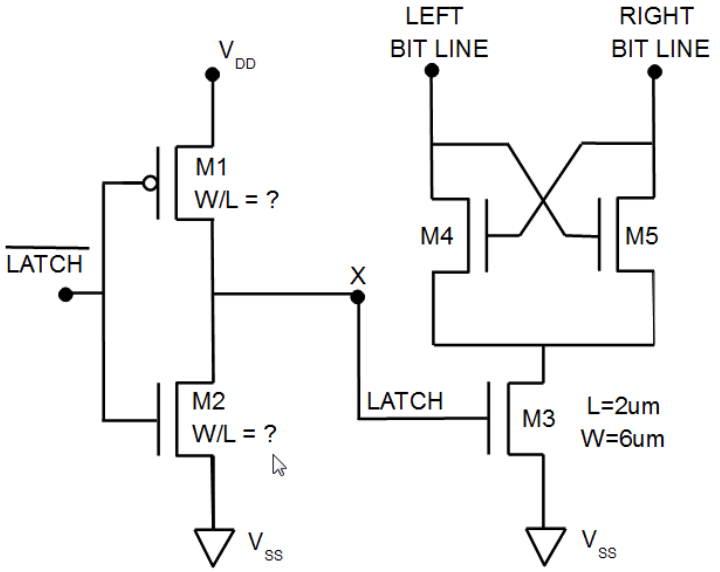

Fig. 5.1

a) Suppose the voltage V_{left} on the left bit line is exactly 2.010 V when LATCH starts to rise, while the voltage V_{right} on the right bit line is 2.000 V. Complete Fig. 5.2 below showing how V_{left} and V_{right} change with time as LATCH rises. Briefly explain your answer. No calculations are necessary. *3 marks*

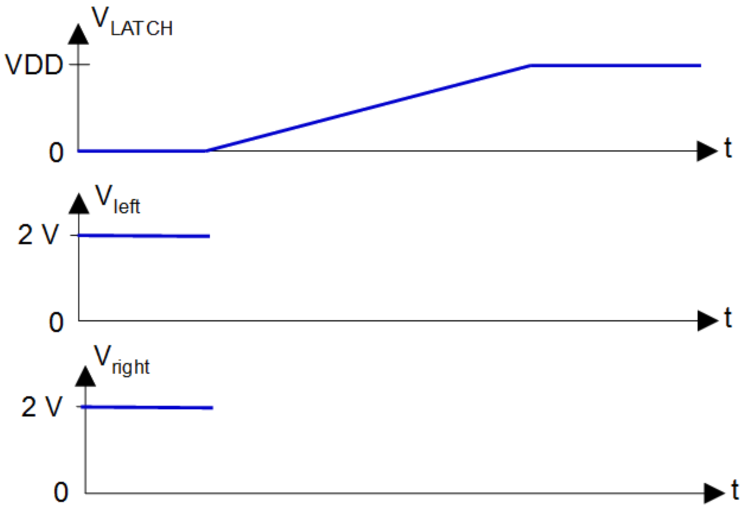

Fig. 5.2

Name: _______________________________

b) For the amplifier to work properly, LATCH must not rise too quickly. Find values for *W*/*L* for M1 and M2 so that the voltage V_{LATCH} at node X rises at 10^8 Vs^{-1} when $\overline{LATCH}$ is 0 and $V_{LATCH} = 1$ V. Ignore source and drain junction capacitances and the capacitance of interconnect lines. The *W*/*L* values should also be chosen so that LATCH is at mid-rail when $\overline{LATCH}$ is at mid-rail. *14 marks*

c) In answering part (b) you should find that very small *W*/*L* ratios are required for M1 and M2. How could you lay out a transistor with very small *W*/*L* while minimizing the total area required for the transistor? You may want to make a sketch to illustrate your answer. *3 marks*

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6. Although it has probably never been done commercially, it is possible to develop a CMOS technology in which the nMOS transistors and pMOS transistors both have p+ poly gates as suggested in Fig. 6.1. This unusual approach might actually give higher performance nMOSFETs compared to conventional technology. In Fig. 6.1, suppose that the substrate is uniformly doped with boron and has 10 Ωcm resistivity. The doping concentration at the surface of the n-well is 10^{16} cm^{-3}. The gate oxide thickness is 25 nm.

a) A threshold adjust implant carried out after gate oxidation and before gate poly deposition is used to set $V_{Tn} = -V_{Tp}$. Which element should be implanted? What dose is required? What value of V_{Tn} results?

15 marks

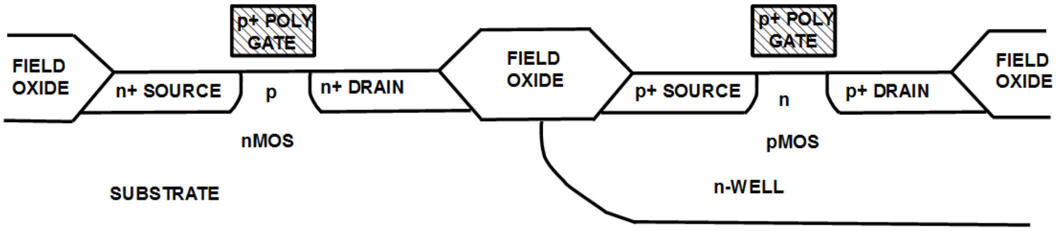

Fig. 6.1

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b) The n-well is formed by implanting phosphorus and then driving in the dopant at 1150°C. At the end of the drive-in the depth of the metallurgical junction between the n-well and the p-type substrate is 4 µm What implant dose should be used to form the n-well? What time is required for the drive-in? *8 marks*

c) What is the sheet resistance of the n-well? *2 marks*

Cross-Section:

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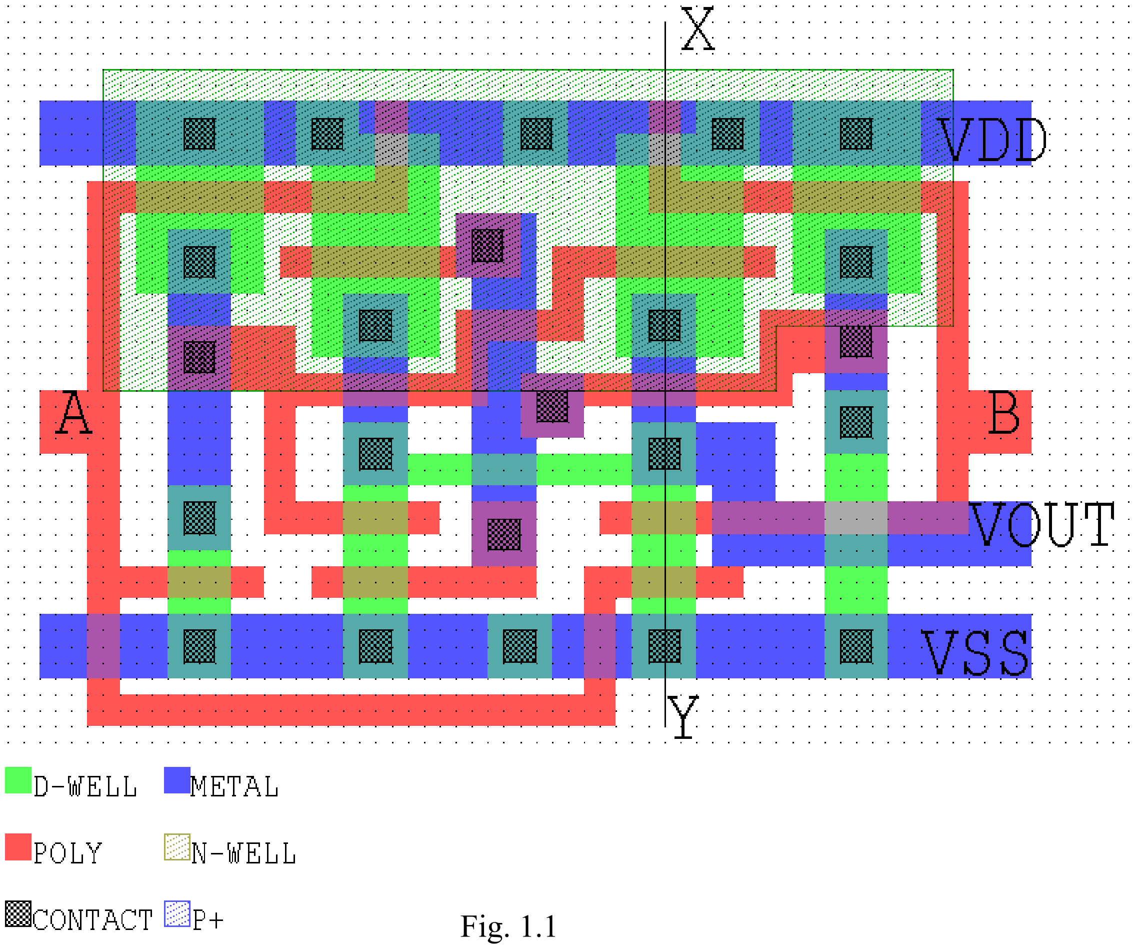

Fig. 1.1

Table 1.1 Truth table for Fig 1.1

A	B	Vout
0	0	
1	0	
0	1	
1	1	

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Equations and Constants

Physical constants: $q = 1.6\text{x}10^{-19}$ C $k = 1.38\text{x}10^{-23}$ JK^{-1} $\varepsilon_0 = 8.85\text{x}10^{-12}$ Fm^{-1} = $8.85\text{x}10^{-14}$ Fcm^{-1}
1eV = $1.6\text{x}10^{-19}$ J $kT/q = 0.0259$ V at room temperature 0°C = 273K

Data for silicon at 300K: $n_i = 10^{10}$ cm^{-3} $E_G = 1.12$ eV $N_C = 2.8\text{x}10^{19}$ cm^{-3} $N_V = 1\text{x}10^{19}$ cm^{-3}
$\varepsilon_s = 11.9\varepsilon_0$ $\mu_n = 1350$ cm^{2}V^{-1}s^{-1} $\mu_p = 480$ cm^{2}V^{-1}s^{-1} $\varepsilon_{ox} = 3.9\varepsilon_0$
in lightly doped material $\mu_n = 1350$ cm^{2}V^{-1}s^{-1} $\mu_p = 480$ cm^{2}V^{-1}s^{-1}

nMOS threshold voltage: $$V_{Tn} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\phi_B + V_{SB})}}{C_{ox}} - \frac{qD_{imp}}{C_{ox}}$$

where $\phi_B = \frac{kT}{q}\ln(\frac{N_A}{n_i})$ and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

pMOS threshold voltage: $$V_{Tp} = V_{FB} - 2\phi_B - \frac{\sqrt{2\varepsilon_s q N_D (2\phi_B + V_{SB})}}{C_{ox}} - \frac{qD_{imp}}{C_{ox}}$$

where $\phi_B = \frac{kT}{q}\ln(\frac{N_D}{n_i})$

Resistivity: $\rho = \frac{1}{q\mu N}$

Saturation drain current: $I_D = \frac{W}{L}\mu_n C_{ox}\frac{(V_{GS} - V_T)^2}{2}$

Triode drain current: $I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$

In the following Q_{impl} is the implanted dopant dose (ions/cm^2):

Drive-in diffusion profile: $C(x) = \frac{Q_{impl}}{\sqrt{\pi D t}} e^{-x^2/(4Dt)}$

Ion implant profile: $C(x) = \frac{Q_{impl}}{\sqrt{2\pi}\,\Delta R_P} e^{-(x-R_P)^2/(2\Delta R_P{}^2)}$

Sheet resistance: $R_S \approx \frac{1}{q\mu\, Q_{impl}}$

Diffusion coefficient: $D = D_0 e^{-E_A/kT}$ ("Intrinsic" diffusion coefficient for lightly-doped material)

Boron: $D_0 = 1.0$ cm^{2}s^{-1} $E_A = 3.5$ eV Phosphorus: $D_0 = 4.7$ cm^{2}s^{-1} $E_A = 3.68$ eV

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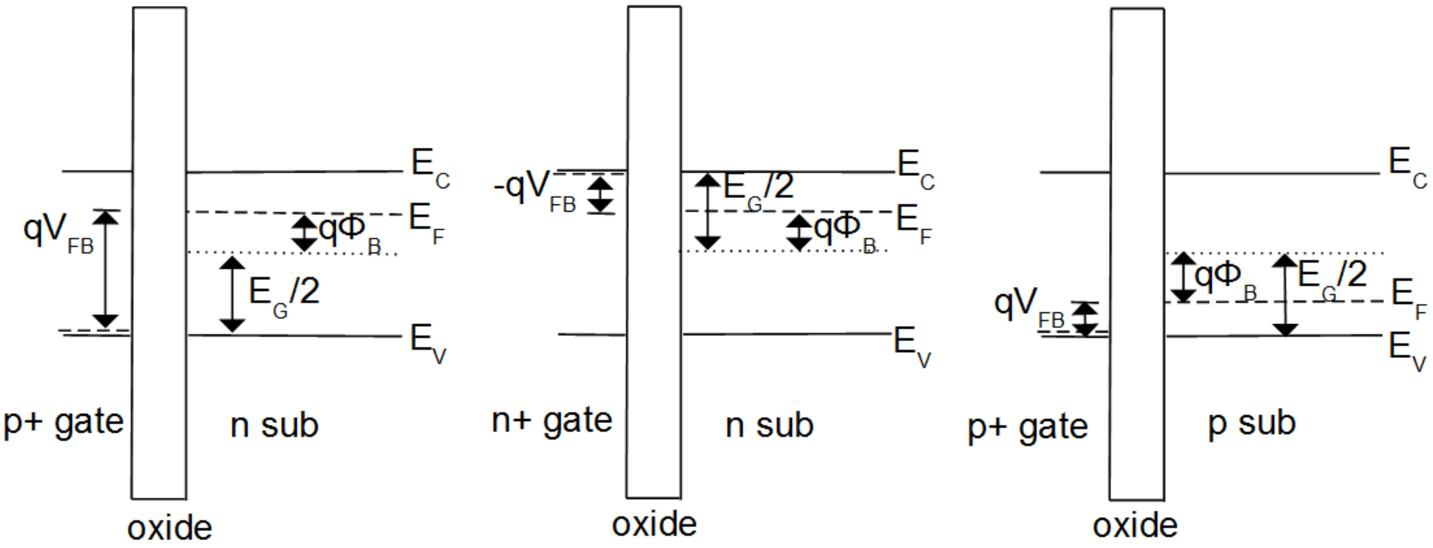
Graphical Data



Diagrams for V_{FB} calculation