7. Fig. 2 shows the circuit diagram for a CMOS inverter. SPICE simulation predicts that the output V_{OUT} of the inverter will briefly "spike" above V_{DD} before dropping to 0 when V_{IN} switches from low to high (see Fig. 3).

   a) Explain why V_{OUT} spikes above V_{DD}.

   6 marks

   b) Explain how the spike in V_{OUT} might trigger latch-up.

   4 marks

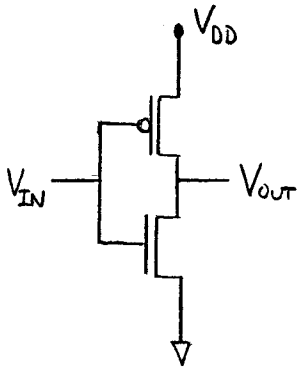

Fig. 2

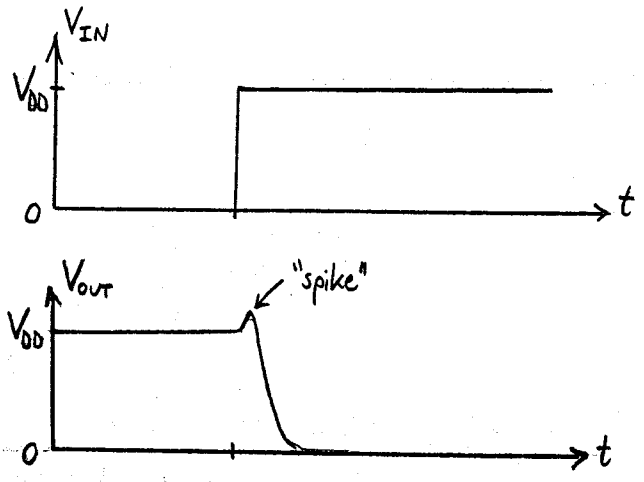

Fig. 3

8. Fig. 4 shows the circuit diagram for a bootstrapped inverter fabricated in Carleton's 97.469 nMOS technology. Calculate the value of $(W/L)_{pd}$ required to give $V_{OUT} = 0.2$ V when $V_{IN} = 5$ V. Assume $V_T = 0.7$ V and ignore the body effect in your calculation. Qualitatively, how would making allowance for the body effect change your answer?

18 marks

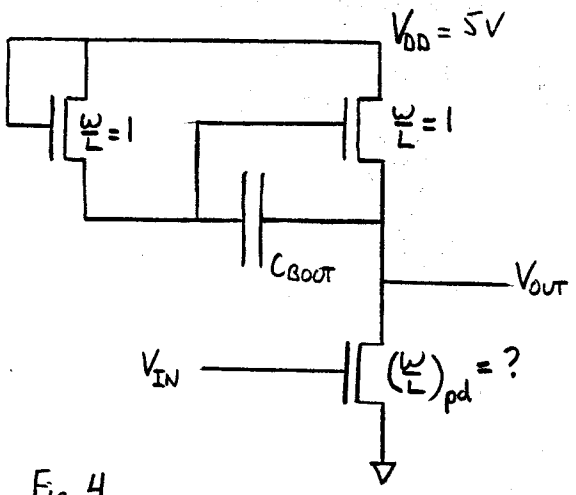

Fig. 4