Name: _____ Student Number: _____

CARLETON UNIVERSITY

FINAL EXAMINATION December 2010

DURATION: 3 HOURS **No. of Students:** 25

Department Name & Course Number: Electronics ELEC 4609

Course Instructor: N.G. Tarr

Authorized memoranda: non-programmable calculators **NO BOOKS OR NOTES**

Students **MUST** count the number of pages in this examination question paper **before** beginning to write, and report any discrepancy immediately to a proctor. This question paper has nine (9) pages.

This examination question paper **may not** be taken from the examination room.

In addition to this question paper, students require: an examination booklet yes ☐ no ☒
a Scantron sheet yes ☐ no ☒

ANSWER ALL QUESTIONS

ALL ANSWERS MUST BE WRITTEN ON THE EXAM PAPER
(If necessary, continue answers on the back of pages)

Physical constants: $q = 1.6\times10^{-19}$ C $k = 1.38\times10^{-23}$ JK^{-1} $\varepsilon_0 = 8.85\times10^{-12}$ Fm^{-1} $= 8.85\times10^{-14}$ Fcm^{-1}
$1eV = 1.6\times10^{-19}$ J $kT/q = 0.0259$ V

Data for silicon at 300K: $n_i = 10^{10}$ cm^{-3} $E_G = 1.12$ eV $N_C = 2.8\times10^{19}$ cm^{-3} $N_V = 1\times10^{19}$ cm^{-3}
$\varepsilon_s = 11.9\varepsilon_0$ $\mu_n = 1350$ cm^{2}V^{-1}s^{-1} $\mu_p = 480$ cm^{2}V^{-1}s^{-1} $\varepsilon_{ox} = 3.9\varepsilon_0$

MOSFET threshold voltage: $$V_T = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_s qN_A(2\phi_B + V_{SB})}}{C_{ox}} - \frac{qD_{imp}}{C_{ox}}$$

nMOSFET saturation drain current ($V_{DS} > V_{GS} - V_T$): $$I_D = \frac{W}{L}\mu_n C_{ox}\frac{(V_{GS} - V_T)^2}{2}$$

nMOSFET triode drain current ($V_{DS} < V_{GS} - V_T$): $$I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$$

1	
2	
3	
4	
5	
6	

Additional equations and data on p. 9

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1. Fig. 1.1 on p. 8 shows the layout of a circuit fabricated in the n-well CMOS technology used in Lab 2. The layout is not complete: the p+ region is not shown. Draw the outline of this region (or regions) on the layout, and use cross-hatching to indicate the interior of the region. (*Note*: In this CMOS technology, by default any area which is not covered by the p+ region receives the n+ implant). *4 marks*

2. In the space provided to the right of the layout in Fig. 1.1, carefully sketch a cross-section through the integrated circuit along line X-Y (i.e., show how the IC would look if cut along line X-Y and viewed from the side). Indicate the n-well and n+ and p+ regions on your cross-section. *16 marks*

3. a) Underneath the layout of Fig. 1.1, draw the circuit schematic corresponding to the layout. Show the substrate (body) connection for each transistor. *10 marks*

b) On the circuit schematic, indicate which transistor(s) may have their threshold voltages modified by the body effect. *2 marks*

c) Determine the W/L ratio for each transistor and write it on the circuit schematic. *2 marks*

d) Complete the truth table below What logic function does the circuit perform?

8 marks

A	B	V_{out}
0	0	
1	0	
0	1	
1	1	

e) Suppose A is held at logic high while B is switched from logic low to logic high and back to logic low. Do you expect V_{out} to exhibit approximately symmetric rise and fall times? Explain. *4 marks*

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4. An analog CMOS circuit requires two capacitors formed between polysilicon and device well, with one capacitor having exactly twice the capacitance of the other under identical bias conditions. Describe the layout approach you would take to producing these two capacitors. Explain how your approach optimizes matching. Make rough sketches of the layout to illustrate your answer. *8 marks*

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5. Consider the depletion load nMOS differential amplifier shown in Fig. 5.1. The amplifier is fabricated in a modified Carleton nMOS technology. $V_T = 0.7$ V for "regular" transistors M1, M2 and M3 while $V_T = -1.2$V for depletion transistors M4 and M5.

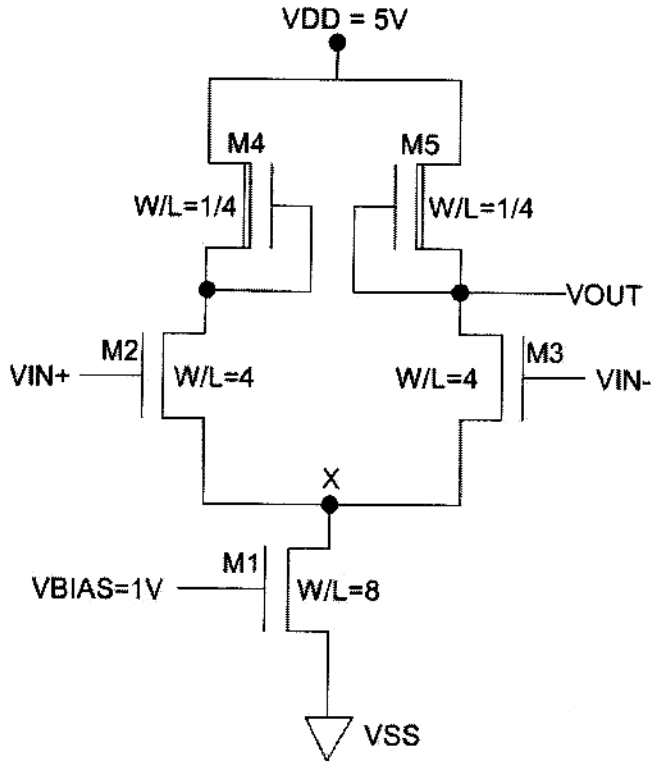

Fig. 5.1 nMOS depletion load differential amplifier

To accurately model the amplifier, the following equation must be used for the drain current in the depletion load transistors in saturation:

$$I_D = \frac{W}{L}\mu_n C_{ox}\frac{(V_{GS}-V_T)^2}{2}[1+\lambda(V_{DS}-V_{DS,sat})]$$

Here $\lambda = 0.1\ V^{-1}$.

a) Assuming that all transistors are in saturation, show that the D.C. value of $V_{out} = 3.8$ V when $V_{in}+ = V_{in}- = 2.5$V. Also find the D.C. voltage at node X. Show your calculations. *4 marks*

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b) Confirm that all transistors are in saturation. *2 marks*

c) Suppose V_{in}- is increased by a small amount ΔV while V_{in}+ is decreased by an equal amount ΔV. Explain why, to a first order approximation, the voltage V_x at node X remains constant. *2 marks*

d) Using the result from part (c), draw a small-signal equivalent circuit for the amplifier. *3 marks*

e) Ignoring the body effect, evaluate the small-signal voltage gain of the amplifier. *10 marks*

f) How would the body effect alter the gain? Explain briefly. No calculations are necessary. *2 marks*

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6. A slightly modified process flow for the ELEC4609 technology is given below. The source/drain junctions are now formed by a phosphorus implant and drive-in rather than by diffusion from a phosphorus vapour source..

Table 6.1: ELEC 4609 5 μm nMOS Process Flow Outline

Starting material: 3 Ωcm p-type (100) orientation

A. Device Isolation

1. Pad oxidation t_{ox}=50 nm T=1100°C time = 1 hour dry O_2
2. Nitride deposition $t_{nitride}$= 80 nm
3. Device well P.E. and nitride etch PE 1
4. Field oxidation t_{ox}=1 μm T=1100°C time= 3 hours wet O_2

B. Active device formation

1. Blanket nitride and pad oxide etchback
2. Gate oxidation t_{ox} = 50 nm T=1100°C time = 1 hour dry O_2
3. Gate polysilicon deposition t_{poly} = 0.4 μm
4. Polysilicon gate P.E. and etch PE 2
5. Gate oxide etchback
6. Source/drain phosphorus implant dose=$5x10^{15}$ cm^{-2} energy=50 keV
7. Implant anneal T=1000°C time = 5 min

C. Contact and Metallization

1. BPSG deposition
2. BPSG flow
3. Contact P.E. and etch PE 3
4. Metal deposition
5. Metal P.E. and etch PE 4

a) Estimate the sheet resistance and metallurgical junction depth for the source and drain regions. State any approximations made in your calculations. *10 marks*

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b) We would like to use ion implantation to set the threshold voltage for active nMOS transistors to 0.7 V (for $V_{SB} = 0$). Indicate where in the process flow the implant should be added. What dopant is required? What dose is required? Suggest a suitable energy for the implant. *15 marks*

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CROSS SECTION:

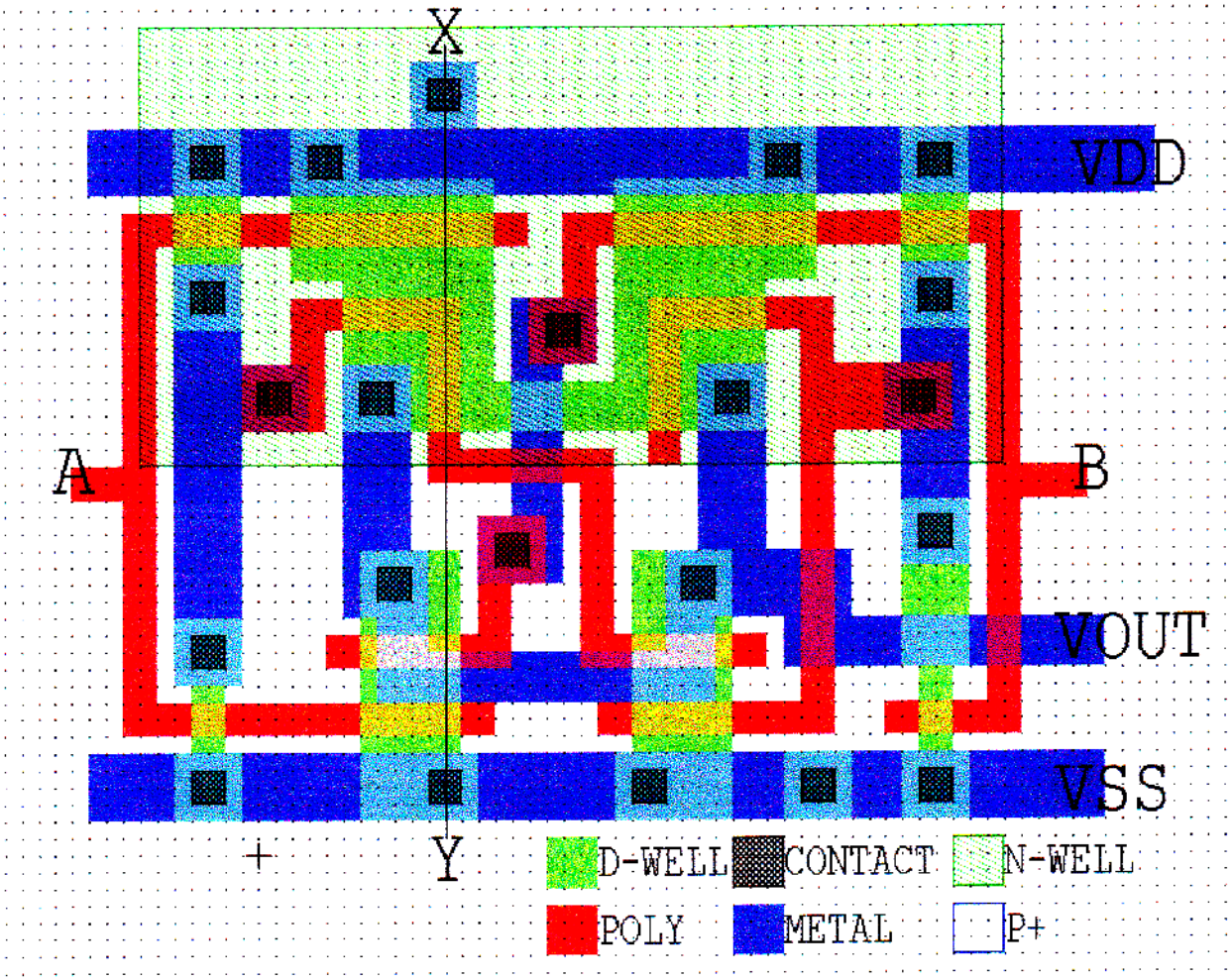

Fig. 1.1 CMOS layout for questions 1, 2, and 3.

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Resistivity: $\rho = \frac{1}{q\mu N}$

ion implant: $C(x) = \frac{Q}{\sqrt{2\pi}\,\Delta R_p} \exp\left(\frac{-(x-R_p)^2}{2\Delta R_p^2}\right)$

drive-in: $C(x) = \frac{Q}{\sqrt{\pi D t}} \exp\left(\frac{-x^2}{4Dt}\right)$

sheet resistance: $R_s = \frac{1}{q\int_0^{x_j} \mu\,(C(x)-C_B)dx} \approx \frac{1}{q\mu\,\overline{Q}}$