Name: _____ Student Number: _____

1. Fig. 1 on p. 5 shows the layout of a logic gate fabricated in the n-well CMOS technology used in Lab 2. The layout is not complete: the p+ regions are not shown. Draw the outline of these regions on the layout, and use cross-hatching to indicate the interior of the regions. (*Note*: In this CMOS technology, by default any region which is not covered by the p+ layer receives the n+ implant). *5 marks*

2. Next to the layout on p. 5, carefully sketch a cross-section through the integrated circuit along line X-Y (i.e., show how the IC would look if cut along line X-Y and viewed from the side). Indicate the n-well and n+ and p+ regions on your cross-section. *17 marks*

3. a) At the bottom of p. 5, draw the circuit diagram corresponding to the layout of Fig. 1. A, B and C are input signals to the gate. Show the connection of the body (well or substrate) terminals on each transistor. *8 marks*

   b) Indicate on the diagram which transistor(s) may have their threshold voltages modified by the body effect as the input signals A, B and C and V_{OUT} change. *3 marks*

   c) Estimate the W/L ratio for each transistor and write it on the circuit diagram. High accuracy is not expected. *3 marks*

   d) Complete the truth table below. Write the Boolean algebra expression for the logic function this circuit performs. *5 marks*

A	B	C	VOUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Boolean expression: V_{OUT} =

4. a) The logic gate of Fig. 1 gives relatively poor immunity to latch-up. Briefly explain why this is so. *4 marks*

   b) Suggest how the layout could be modified to greatly improve latch-up immunity. You may wish to make a sketch to illustrate your answer, but you do not need to redraw the entire layout. Explain how your modifications help resist latch-up. *4 marks*