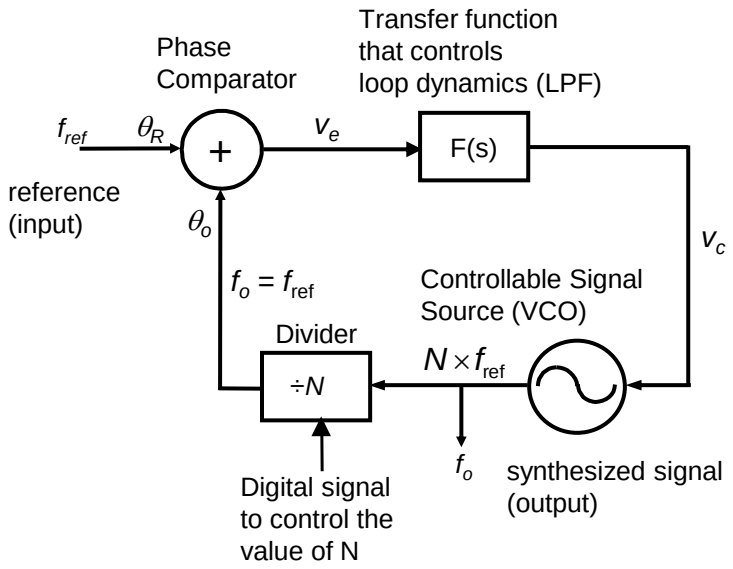
RF Systems Course: PLL Lecture I

Basic Phase Locked Loop (PLL) Operation

- Many ways to make a freq synthesizer, but PLL based is very common.
- Can have either integer N or frac N but most of this lecture will work for both.
- Integer N is simpler, so we start with it.
- PLL is a feedback system compares phase of a reference to phase of divided down VCO signal.
- Feedback forces these signals to be equal.

$$f_o = N \cdot f_{\text{ref}}$$

- We use phase so no finite freq error.
- Reference is a quartz crystal
- very accurate, but can't make at high freq or make tunable.



PLL Components VCOs and Dividers

- VCO has an output freq which depends on an input voltage.
- Generally we assume it is linear but really it never is.

$$\omega_o = \omega_{\text{nom}} + \omega_{\text{VCO}} = \omega_{\text{nom}} + K_{\text{VCO}} v_c$$

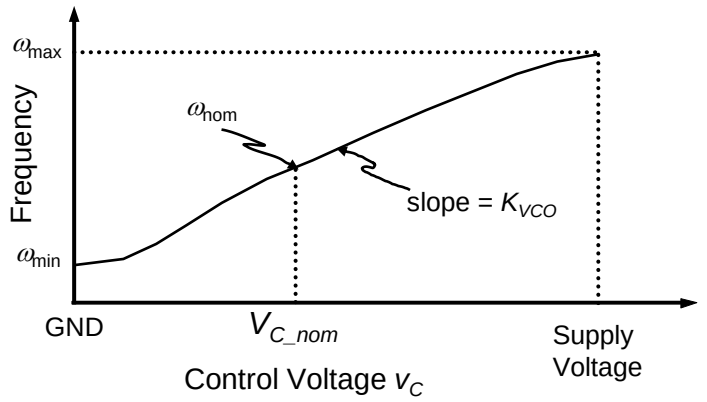
- Since phase and freq are related by $\omega = \dfrac{d\theta}{dt}$
- We note that

$$\theta_{\text{VCO}} = \int \omega_{\text{VCO}}\, dt = K_{\text{VCO}} \int_0^t v_c(\tau) d\tau$$

- We will do a lot of analysis in Laplace domain so:

$$\frac{\theta_{\text{VCO}}(s)}{v_c(s)} = \frac{K_{\text{VCO}}}{s}$$

- For a divider we also note that: $\dfrac{\theta_o}{v_c} = \dfrac{1}{N} \cdot \dfrac{K_{\text{VCO}}}{s}$

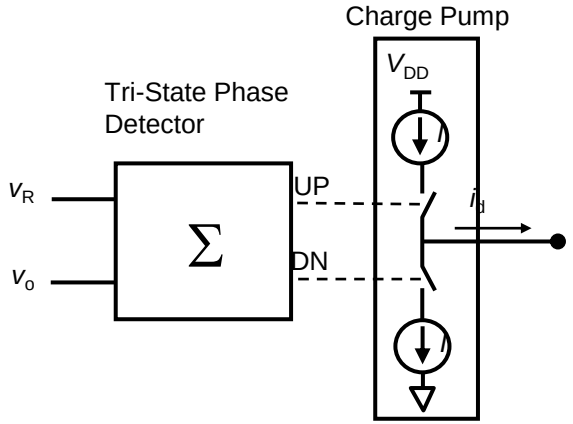


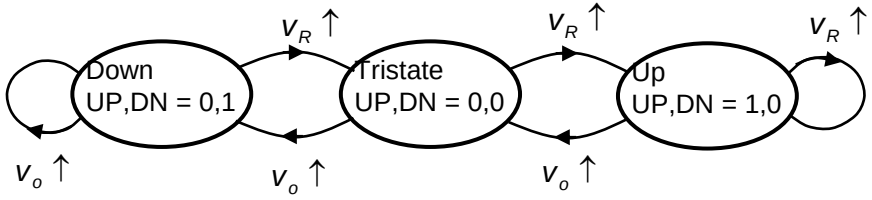
PLL Components: Phase Detectors

- Phase detector produces output proportional to phase difference of two input signals.

$$v_e(s) = K_{\text{phase}}\left(\theta_R(s) - \theta_o(s)\right)$$

- equation is linear -> may not hold over all phase differences.
- Typical tri-state phase detector shown at the right.
- It responds to rising edges that cause it to change state and produce UP and DN signals that control two current sources.





PLL Components: Phase Detectors

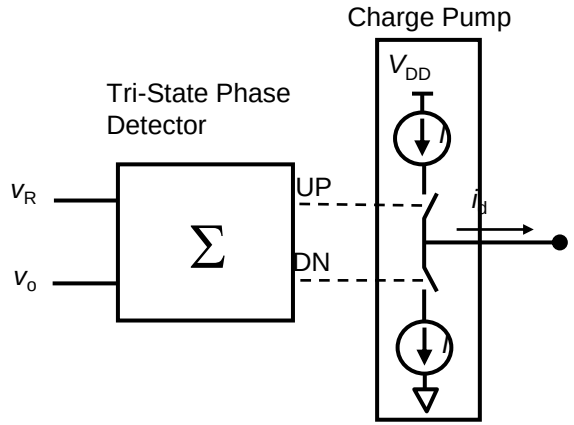
- If a rising edge of v_o is received -> VCO too fast -> DN pulse generated until v_r arrives.
- If a rising edge of v_r is received -> VCO too slow -> UP pulse generated until v_o arrives.
- If currents have a value of I then average output current is:

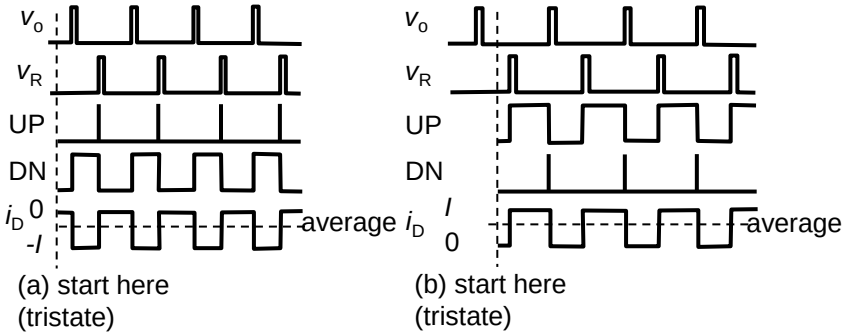
$$i_d = I\frac{\tau}{T} = \left(\frac{I}{2\pi}\right)(\theta_R - \theta_o)$$

- phase detector gain is:

$$K_{\text{phase}} = \frac{I}{2\pi}$$

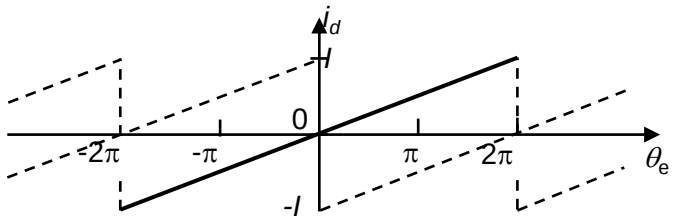
- Note responds to edges so waveform shape not that important.

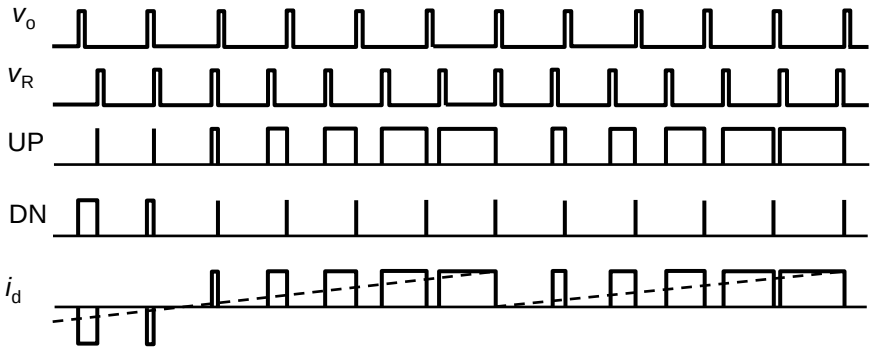




PLL Components: Phase Detectors

- Note that for every given phase difference there is always two interpretations depending on when phase detector was started.
- Also note that phase detector is only linear for a limited range after which there is a nonlinear event!
- What if signals are at two different freqs?
- Turns out it will act like a freq detector as well no matter where you start it.
- Output will then push VCO in the right direction to try and make freqs equal.

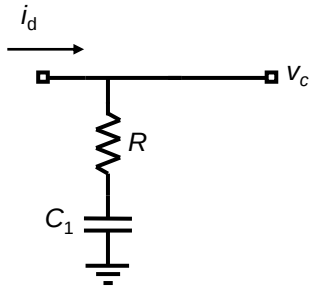




PLL Components: The Loop Filter

- Loop filter typically an RC network that accepts current as input and produces voltage as output.
- transfer function is an impedance
- For typical filter shown at the right:

$$Z = R + \frac{1}{sC_1}$$

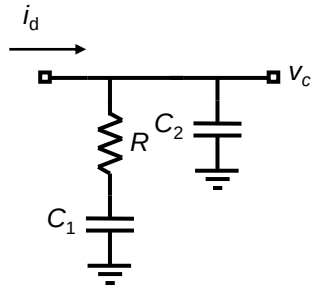


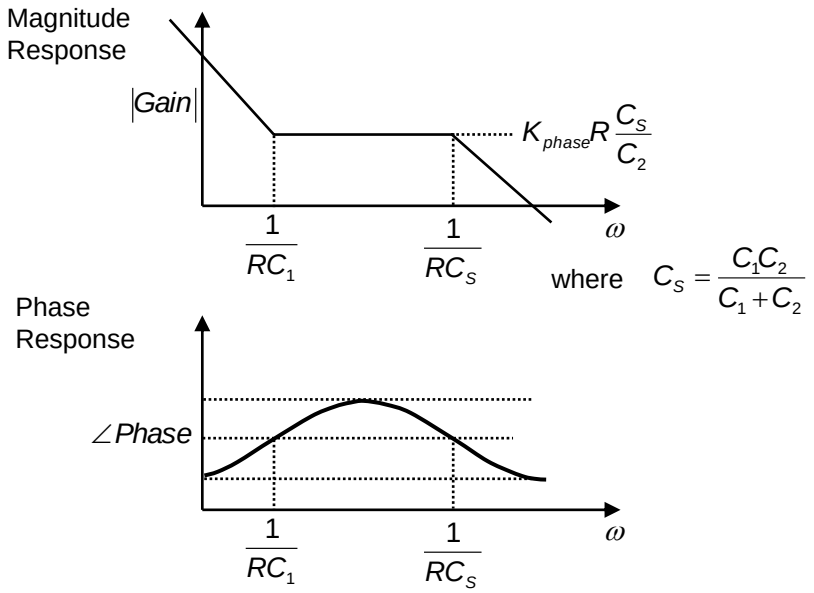
- Therefore the output can be found as

$$v_c = Zi_d$$

PLL Components: The Loop Filter

- Often to provide more attenuation at higher freqs 2nd cap is added that is much smaller than C_1
- With that cap freq response of filter is plotted below:





Continuous-Time Analysis of PLLs

- We now have s domain eqs for all the blocks that make up the system.
- Assuming that: $$F(s) = R + \frac{1}{sC_1} = \frac{sC_1R + 1}{sC_1}$$
- transfer function for the loop is:

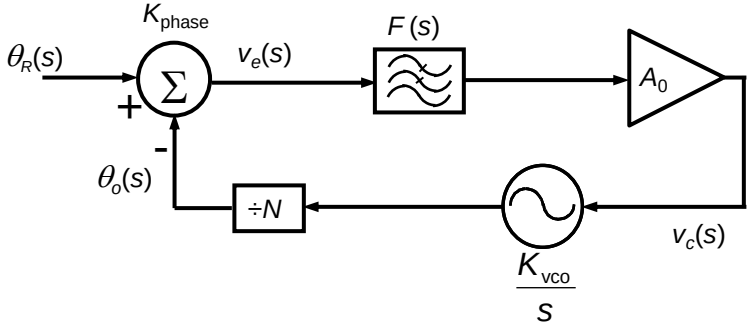
$$\frac{\theta_o}{\theta_R} = \frac{\frac{IK_{VCO}}{2\pi \cdot N}\left(R + \frac{1}{sC_1}\right)}{s + \frac{IK_{VCO}}{2\pi \cdot N}\left(R + \frac{1}{sC_1}\right)} = \frac{\frac{IK_{VCO}}{2\pi \cdot NC_1}(RC_1s + 1)}{s^2 + \frac{IK_{VCO}}{2\pi \cdot N}Rs + \frac{IK_{VCO}}{2\pi \cdot NC_1}}$$

This system has a natural freq and damping constant:

$$\omega_n = \sqrt{\frac{IK_{VCO}}{2\pi \cdot NC_1}} \qquad \zeta = \frac{R}{2}\sqrt{\frac{IK_{VCO}C_1}{2\pi \cdot N}}$$

This can also be written as:

$$C_1 = \frac{IK_{VCO}}{2\pi \cdot N\omega_n^{\,2}} \qquad R = 2\zeta\sqrt{\frac{2\pi \cdot N}{IK_{VCO}C_1}} = \zeta\frac{4\pi \cdot N\omega_n}{IK_{VCO}}$$

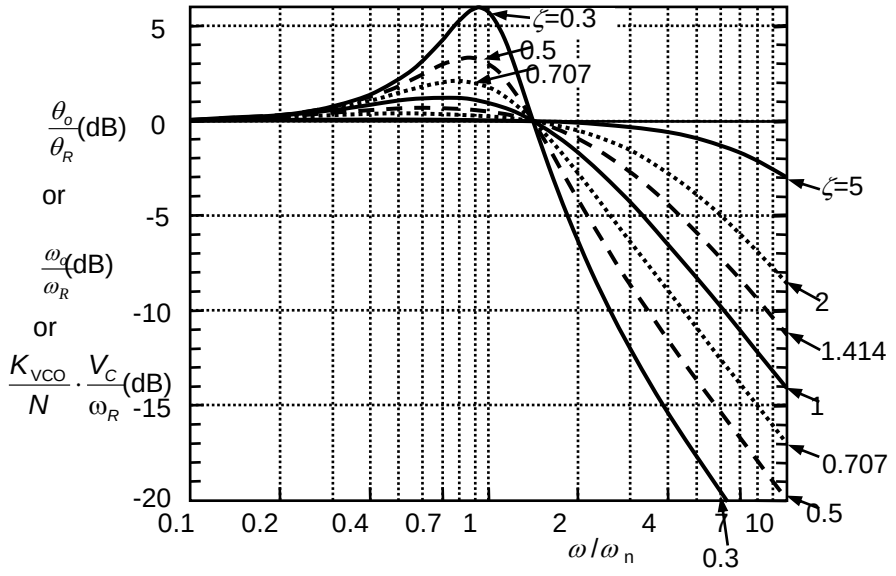


- Sometimes it is more useful to have an eqn for control voltage because that is what we can see easily in simulation:

$$\frac{V_C}{\omega_R} = \frac{\frac{N\omega_n^{\,2}}{K_{VCO}}\left(\frac{2\zeta}{\omega_n}s + 1\right)}{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}}$$

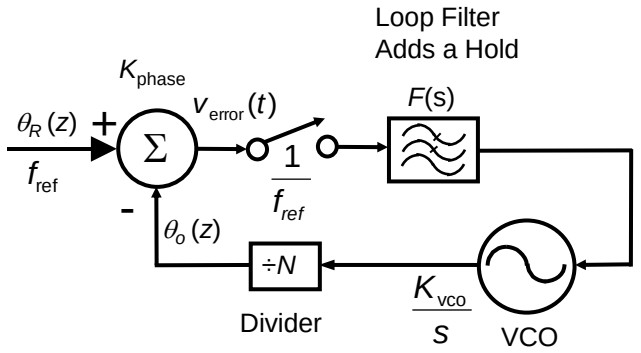
Continuous-Time Analysis of PLLs

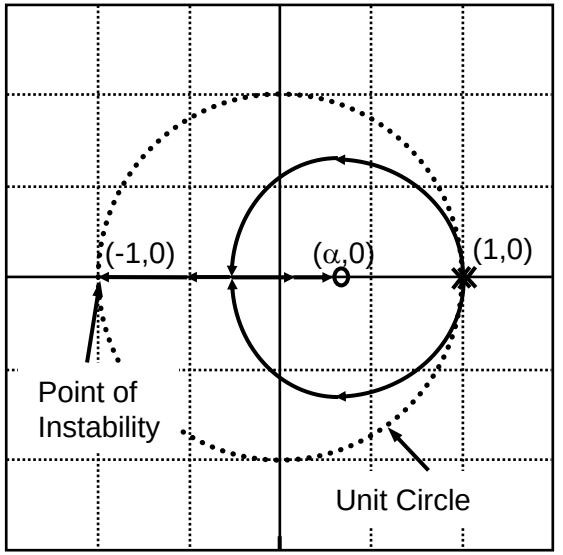
- freq response of loop.
- below the natural freq, loop has gain and output phase will track input phase as intended.
- Above natural freq, loop has less and less effect so more and more the phase of the VCO has no relationship to the phase of the reference.



Discrete Time Analysis for PLL

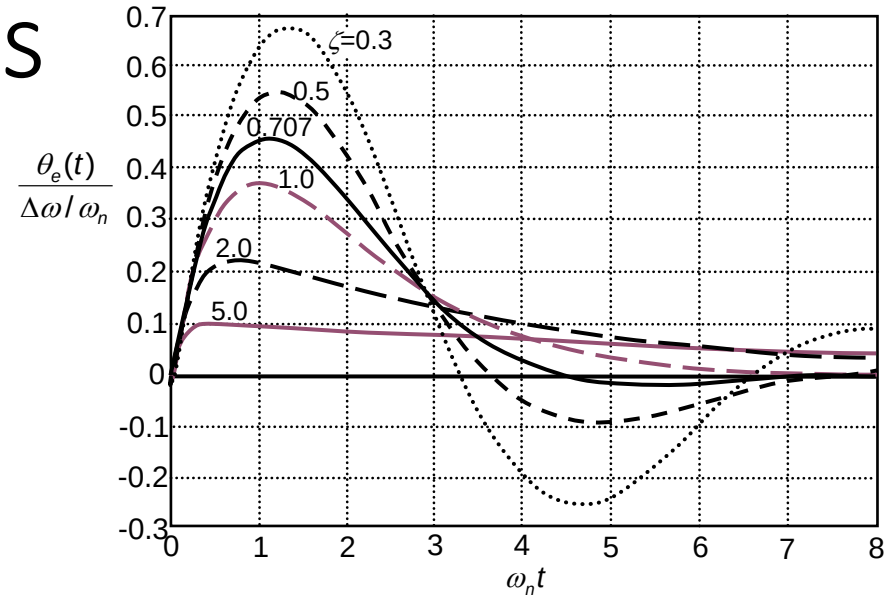
- model of a PLL in s domain breaks down if things start changing at a significant fraction of reference freq.
- Since loop only “updates” once every reference period, in order for it to approximate continuous behaviour not much can change over that interval.
- This is guaranteed by choosing a loop BW which is small fraction (less than 1/10th) of the reference freq.
- If we fail to do this, loop can become unstable even if s domain poles are all in left hand plane.
- There is some detailed analysis in the book which isn’t that important for the RF systems course.

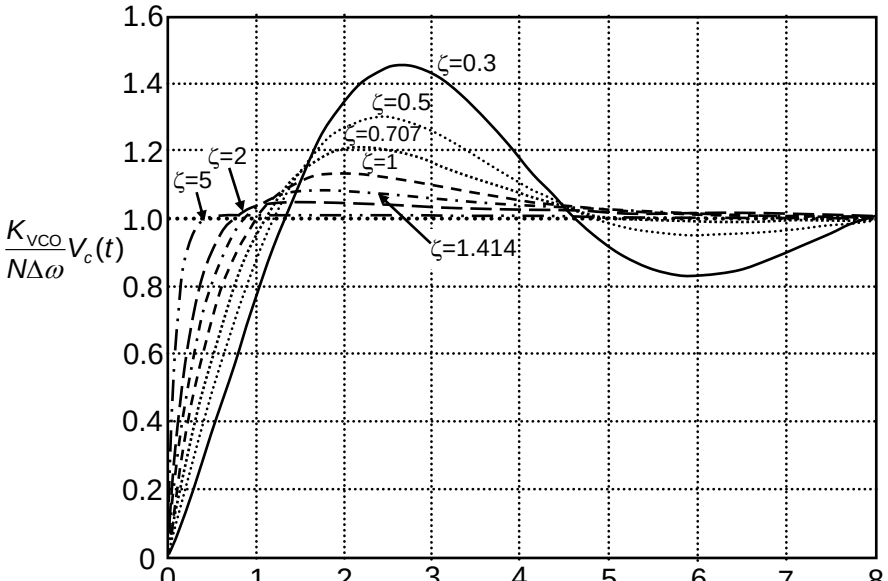




Transient Behavior of PLLs

- We can take inverse Laplace transform of previous loop eqns to get eqns for transient response.
- eqns are given in the book and results are plotted on the right.
- Note phase always returns to zero (there are 2 integrators in the loop) while control voltage settles to a new normalized value as expected.
- This is a linear response and only holds if phase detector and other components remain well modeled by their linear eqns.





Example of Limits of Theory So Far

- Assume damping const. = 0.707, 3dB BW = 150kHz.
- What is max freq step at input such that theory will still work? How long to settle under this condition?

$$\omega_n \approx \frac{\omega_{3dB}}{(1+\zeta\sqrt{2})} = \frac{2\pi \cdot 150kHz}{2} = 2\pi \cdot 75kHz$$

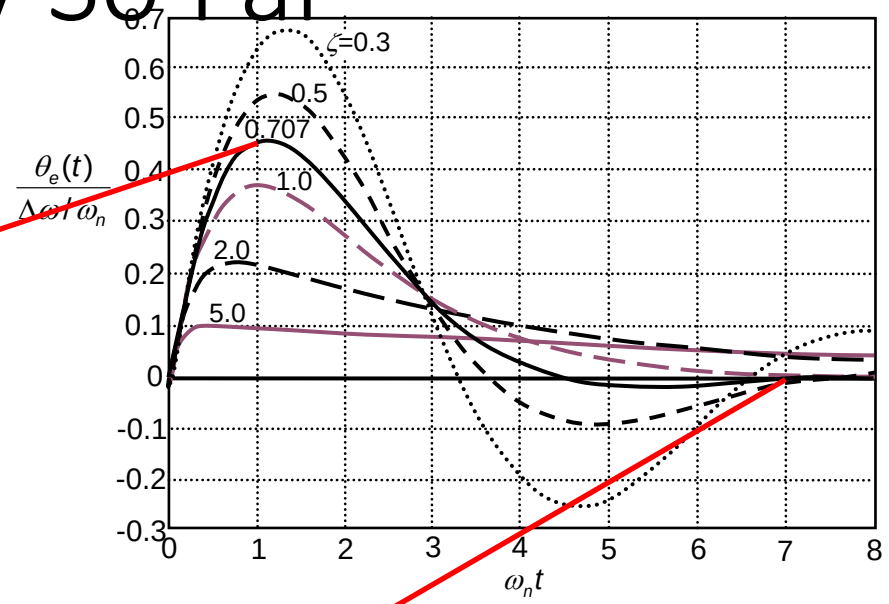
- max normalized phase error is 0.46 so max phase error is:

$$\theta_{e\_max} = 0.46\frac{\Delta\omega}{\omega_n}$$

- max phase error that PFD can withstand is 2π
- Largest freq step system can handle is:

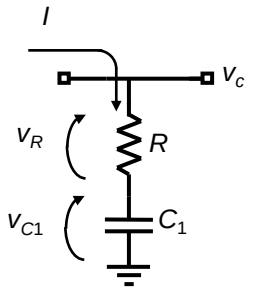
$$\Delta\omega_{max} = \frac{\theta_{e\_max}\omega_n}{0.46} = \frac{2\pi(2\pi \cdot 75kHz)}{0.46} = \frac{6.43Mrad}{s} = 1.02MHz$$

  - If freq step bigger than this, PLL will lose lock and cycle slip.
  - Trans resp will look different than shown.
  - Here will take till $\omega_n t = 7$ for PLL to settle or 14.9µs.



Nonlinear Transient Behaviour

- If a larger freq step is experienced PLL will “cycle slip” and have to re-acquire lock.
- In this case PFD will push VCO back in the right direction but it will be operating as a freq detector for a while.
- If we assume that CP is on roughly half the time: $\frac{\Delta v_C}{\Delta t} = \frac{I}{2C_1}$
- Solving for settling time: $\frac{\Delta v_C}{\Delta t} = \frac{I}{2C_1}$

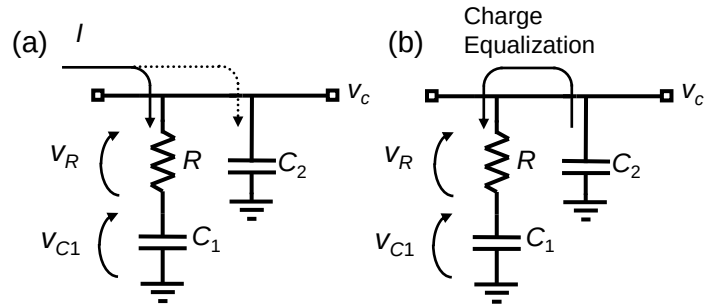


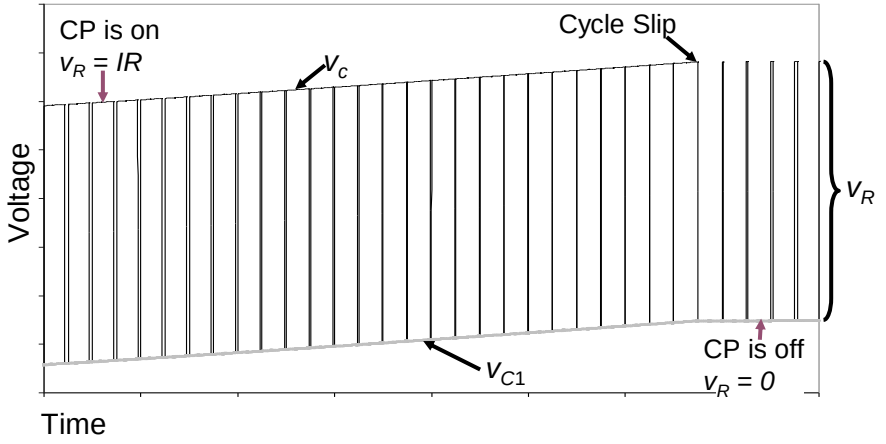
Some more math equivalents yields:

$$T_s = \frac{2C_1 \Delta\omega N}{IK_{\text{VCO}}} = \frac{\Delta\omega}{\pi\omega_n^{\ 2}}$$

Nonlinear Transient Behaviour

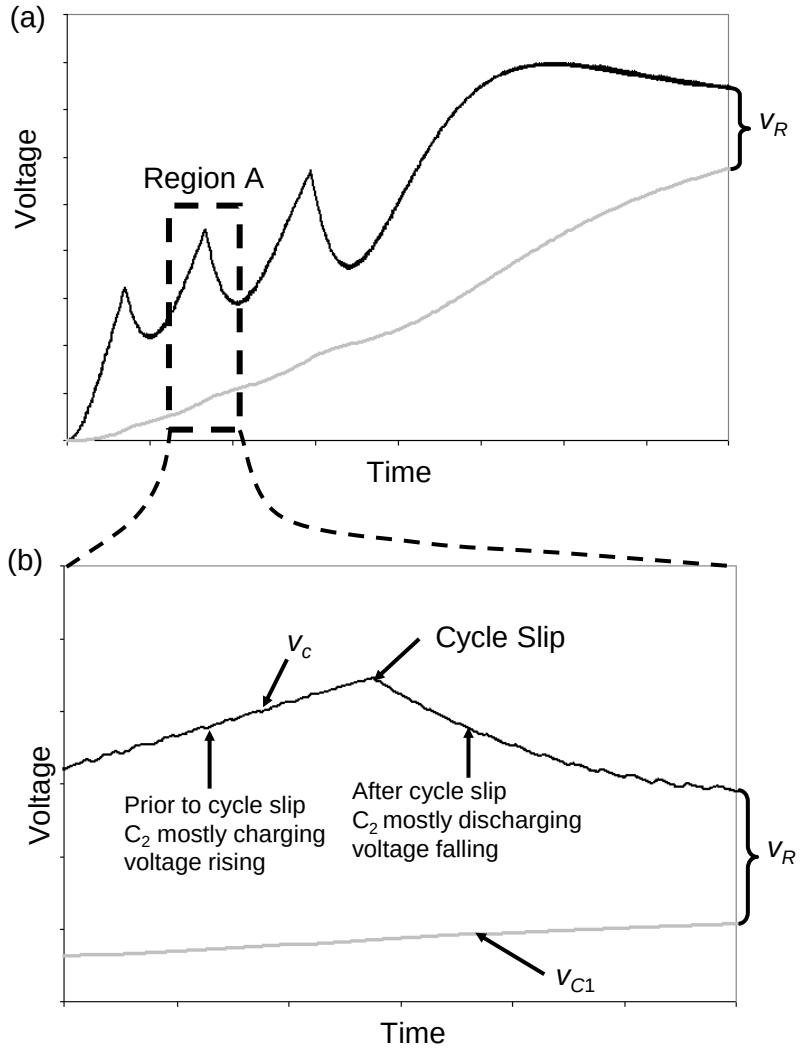
- PLL will have 2 modes (CP on) means current is being pushed onto C_1 and C_2, and CP off where charge equalization happens between the 2 caps.
- At cycle slip CP goes from being on almost all the time to off almost all the time.





Nonlinear Transient Behaviour

- This is a more zoomed out look at a PLL that is acquiring lock.
- looking at the loop filter voltage.
- There are three cycle slips in the example.
- C_2 “smooths out” the behaviour so voltages don’t try and change instantly.



Example of Estimation of Settling Times

- 3.7-4.3GHz synth with step size of 1MHz
- 40MHz XTAL, CP with $2\pi \cdot 100\mu A$ of output current, VCO with 3V supply are available
- Design frac N synth with loop BW = 150kHz
- Estimate settling time for 30MHz and 300MHz freq step.

- VCO operating with 3V supply must have 600MHz tuning range -> K_{VCO} ~ 200MHz/V.
- For CP K_{phase} = 100µA/rad
- VCO freq 4GHz, reference freq 40MHz -> division ratio 100.
- 3dB freq of 150kHz for loop requires natural freq of 75kHz.

$$C_1 = \frac{IK_{\mathrm{VCO}}}{2\pi \cdot N{\omega_n}^2} = \frac{2\pi \cdot 100\mu A \cdot (2\pi \cdot 200MHz/V)}{2\pi \cdot 100(2\pi \cdot 75kHz)^2} = 5.66nF$$

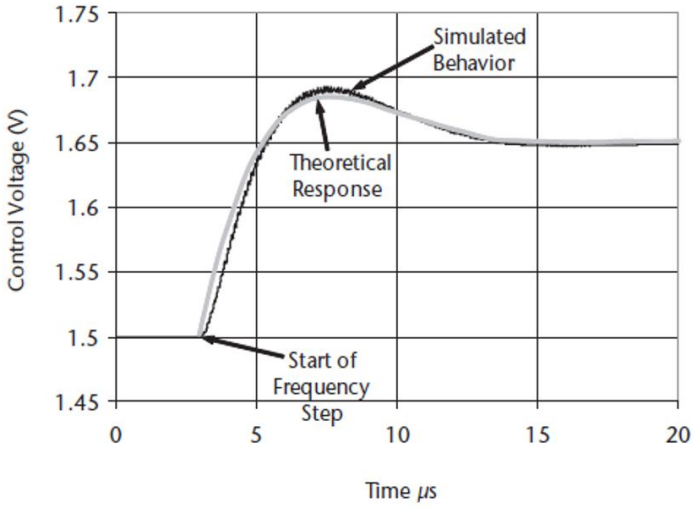
- Need damping const. -> choose 0.707

$$R = 2\zeta\sqrt{\frac{2\pi \cdot N}{IK_{\mathrm{VCO}}C_1}} = \left(\frac{2}{\sqrt{2}}\right)\sqrt{\frac{2\pi \cdot 100}{2\pi \cdot 100\mu A\left(2\pi \cdot \frac{200MHz}{V}\right) \cdot 5.66nF}} = 530\Omega$$

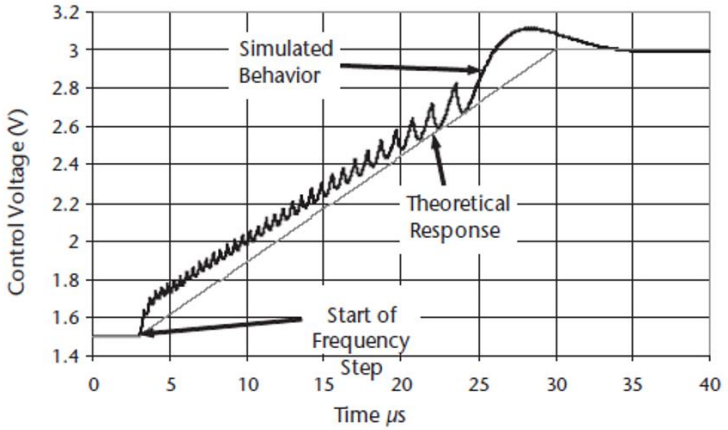
- Set C_2 = 566pF (1/10th C_1)
- Output freq step of 30MHz and 300MHz corresponds to input step of 0.3MHz and 3MHz.
- From previous example can tolerate 1MHz input step without cycle slip.
- So for 30MHz step expect 15µs as before.
- 2nd case will have cycle slip so acquisition time is:

$$T_s = \frac{\Delta\omega}{\pi{\omega_n}^2} = \frac{2\pi \cdot 3MHz}{\pi(2\pi \cdot 75kHz)^2} = 27\mu s$$

- Complete settling will be $27\mu s$ plus $15\mu s$ for phase lock.
- Can simulate this with a circuit simulator using behavioural blocks.



Response of the PLL design's control voltage during a 30-MHz frequency step.



Response of the PLL design's control voltage during a 300-MHz frequency step.

Various Noise Sources in PLLs

- VCO noise $\varphi^2_{\mathrm{VCO}}(\Delta\omega) = \dfrac{C}{\Delta\omega^2} + D$

- Crystal reference noise

$$\varphi^2_{XTAL}(\Delta\omega) = 10^{-16\pm1} \cdot \left[1 + \left(\frac{\omega_0}{2\Delta\omega \cdot Q_L}\right)^2\right]\left[1 + \frac{\omega_c}{\Delta\omega}\right]$$

- Frequency divider noise

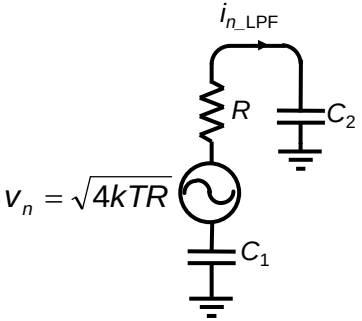
$$\varphi^2_{\mathrm{Div\_Added}}(\Delta\omega) \approx \frac{10^{-14\pm1} + 10^{-27\pm1}\omega_{\mathrm{do}}^2}{2\pi \cdot \Delta\omega} + 10^{-16\pm1} + \frac{10^{-22\pm1}\omega_{\mathrm{do}}}{2\pi}$$

- Phase detector noise

- Charge pump noise $\varphi^2_{\mathrm{PD}}(\Delta\omega) \approx \dfrac{2\pi \cdot 10^{-14\pm1}}{\Delta\omega} + 10^{-16\pm1}$

- Loop filter noise

$$i_{n\_\mathrm{LPF}} = \frac{1}{R} \cdot \frac{v_n s}{s + \dfrac{C_1 + C_2}{C_1 C_2 R}} \approx \frac{1}{R} \cdot \frac{v_n s}{s + \dfrac{1}{C_2 R}}$$



- ΣΔ noise

$$\frac{\varphi^2_{\Sigma\Delta}(f)\ [\mathrm{rad}^2/\mathrm{Hz}]}{2} = \frac{(2\pi)^2}{24 f_r} \cdot \left[2\sin\left(\frac{\pi f}{f_r}\right)\right]^{2(m-1)}$$

$$PN_{\Sigma\Delta}(f)\ [\mathrm{dBc/Hz}] = 10\log\left\{\frac{(2\pi)^2}{24 f_r} \cdot \left[2\sin\left(\frac{\pi f}{f_r}\right)\right]^{2(m-1)}\right\}$$

In Band and Out of Band Noise

- Whether noise is LPF or HPF depends on where in the loop it is injected. Most noise is LPF:

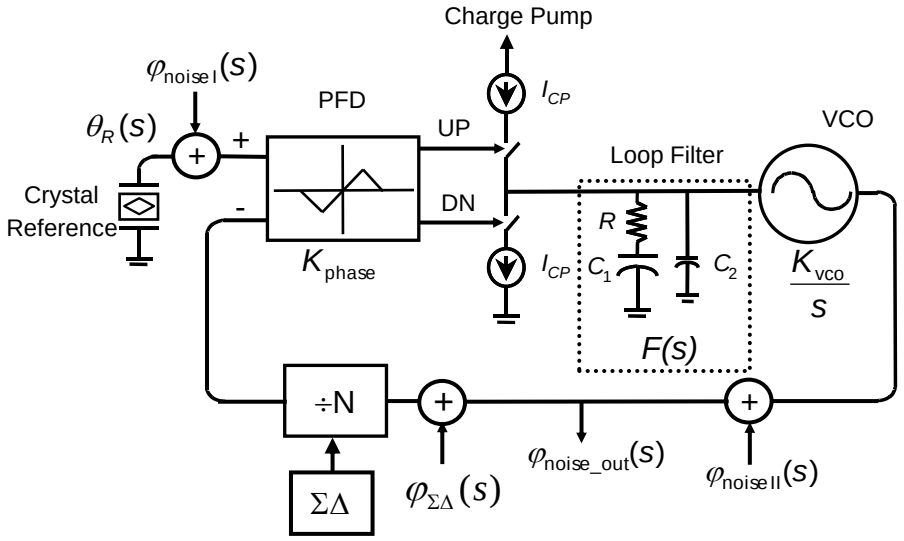
$$\frac{\varphi_{\text{noiseout}}(s)}{\varphi_{\text{noiseI}}(s)} = \frac{\frac{IK_{\text{VCO}}}{2\pi \cdot C_1}(1 + RC_1 s)}{s^2 + \frac{IK_{\text{VCO}}}{2\pi \cdot N} Rs + \frac{IK_{\text{VCO}}}{2\pi \cdot NC_1}}$$

- VCO noise is HPF:

$$\frac{\varphi_{\text{noiseout}}(s)}{\varphi_{\text{noiseII}}(s)} = \frac{s^2}{s^2 + \frac{IK_{\text{VCO}}}{2\pi \cdot N} Rs + \frac{IK_{\text{VCO}}}{2\pi \cdot NC_1}}$$

- $\Sigma\Delta$ noise has its own transform but is also LPF

$$\frac{\varphi_{\text{noise\_out}}(s)}{\varphi_{\Sigma\Delta}(s)} = \frac{K_{\text{VCO}} K_{\text{phase}}(1 + sC_1 R)}{s^2 N(C_1 + C_2)(1 + sC_s R) + K_{\text{VCO}} K_{\text{phase}}(1 + sC_1 R)}$$



Example Phase Noise Calculations

- Continue with same specs as previous examples.
- VCO has PN = -120dBc/Hz @ 1MHz offset (bottoms at -130dBc/Hz), CP noise current = 10pA/$\sqrt{Hz}$
- Ignore all other noise what does PN plot look like? What if you needed to do this with only integer N?

- With Int N to get a step size of 1MHz need 1MHz reference so in that case N = 4000.
- With loop BW of 150KHz and damping const of 0.707 get C1 =141.5pF and R =21.2kΩ.
- will assume VCO falls at 20dB/decade thus VCO PN is:

$$C = log^{-1}\left(\frac{PN_{VCO}}{10}\right)\cdot\Delta\omega^2 = log^{-1}\left(\frac{-120}{10}\right)\cdot(2\pi\cdot 1MHz)^2 = 39.5\frac{rad^4}{Hz^2}$$

- VCO bottoms at -130dBc/Hz :

$$D = log^{-1}\left(\frac{PN_{VCO}}{10}\right) = log^{-1}\left(\frac{-130}{10}\right) = 10^{-13}\frac{rad^2}{Hz}$$

$$\phi^2_{\text{VCO}}(\Delta\omega) = \sqrt{\frac{39.5}{\Delta\omega^2}+10^{-13}}\frac{rad}{\sqrt{Hz}}$$

- noise from CP can be input referred by dividing by K_{Phase}

$$Noise_{CP} = \frac{i_n}{K_{Phase}} = \frac{10\frac{pA}{\sqrt{Hz}}}{100\frac{\mu A}{rad}} = 100n\cdot\frac{rad}{\sqrt{Hz}}$$

- Noise from the loop filter also moved back to input:

$$Noise_{LF}(\omega) = \frac{1}{K_{Phase}}\left|\frac{\sqrt{\frac{4kT}{R}}j\omega}{j\omega+\frac{1}{C_2R}}\right|$$

- Now need to transfer all noise to the output using appropriate TF

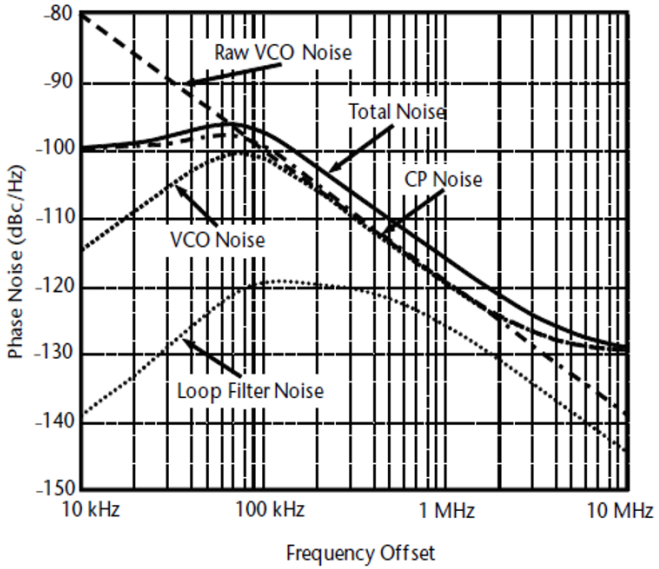
$$\phi_{\text{noise out\_CP}}(s) = \frac{2.22\cdot 10^{13}(1+3\cdot 10^{-6}s)}{s^2+6.66\cdot 10^5 s+2.22\cdot 10^{13}}100n\cdot\frac{rad}{\sqrt{Hz}}$$

- To plot PN in dBc/Hz:

$$PN_{\text{CP}}(\Delta\omega) = 20log\left(\left|\frac{2.22\cdot 10^{13}(1+3\cdot 10^{-6}j\Delta\omega)}{j\Delta\omega^2+6.66\cdot 10^5 j\Delta\omega+2.22\cdot 10^{13}}\right|100n\cdot\frac{rad}{\sqrt{Hz}}\right)$$

- Others done in similar way.
- To get total noise:

$$\phi_{\text{total}} = \sqrt{\phi_{\text{noise out\_CP}}{}^2+\phi_{\text{noise out\_VCO}}{}^2\phi_{\text{noise out\_LPF}}{}^2}$$

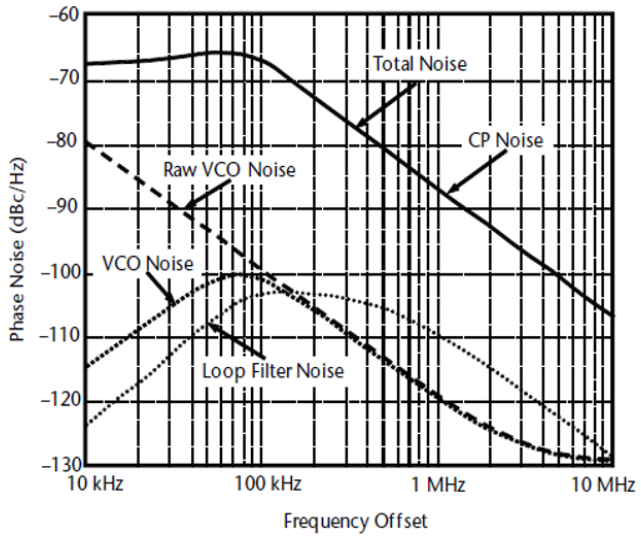


Example Phase Noise Calculations

- Now can compute int PN:

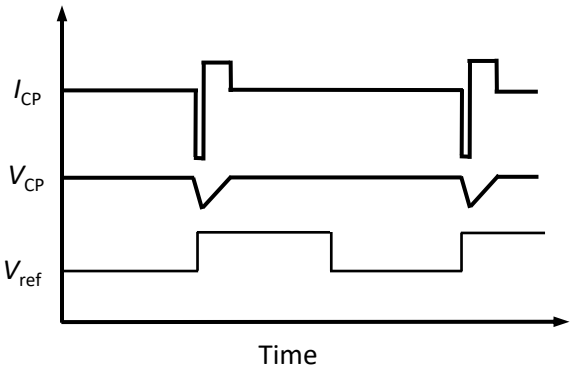
$$IntPN_{rms} = \frac{180\sqrt{2}}{\pi}\sqrt{\int_{f=10kHz}^{f=10MHz} \phi_{\text{total}}{}^2 df} = 0.41$$

- Using integer N specs results look like:



- Large division ratio clearly blows up in band noise!
- Clearly shows why you want frac N!

PLL Reference Feedthrough



- If CP up and down currents aren't equal can cause constant correction even in the locked state.
- E.g. charge is added, creating a phase error that then needs to be removed next cycle.
- This causes spurs at the reference frequency to get modulated onto the VCO output.