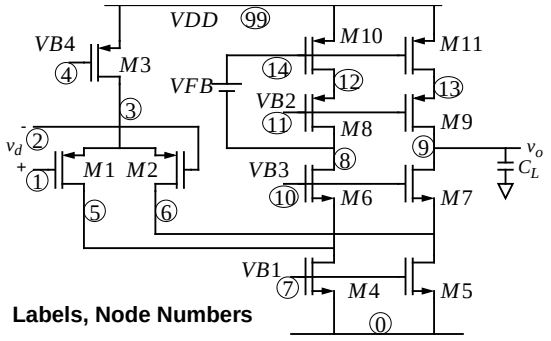
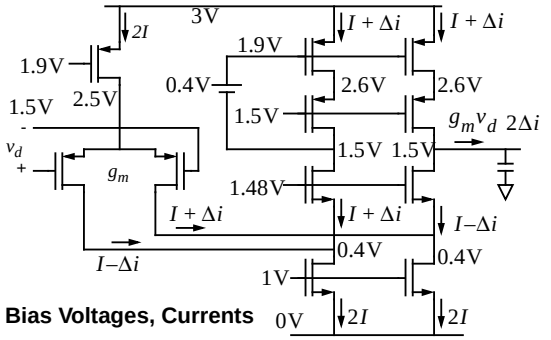
PMOS Input Folded Cascode Amplfier Design Example

Starting point: Slew rate required 100V/μsec=I/C. For C=2pF, require 200 μA (equal to 2I on schematic), which sets current through M3,M4,M5. Then I10,11 should be 100 μA. To size transistors, choose Von, e.g., 0.2V and a safe VDS slightly larger, e.g., 0.4 V. Reminder, Von =VGS-VT is the minimum possible VDS.



Labels, Node Numbers



Bias Voltages, Currents

Again, if v_{on} = 0.2 V, and V_{TN} = 0.8V, V_{TP} = –0.9V, V_{GSN} = 1.0 V, $|V_{GSP}|$ = 1.1 V. For safe margin, let $V_{DS} = V_{on} + 0.2\text{V} = 0.4\text{V}$. V_{DD} = 3 V, (bias voltages shown left). Again, swing from about 0.6 V to 2.4 V. Estimate: K_{pn} = 75 μA/V, K_{pp} = 25 μA/V, $\lambda_{n,p}$ = 0.2 for L = 2 μm, $\lambda_{n,p}$ = 0.5 for L = 0.8 μm

$$I_{DS} = \frac{K_p}{2}\frac{W}{L}v_{on}^2(1+\lambda V_{DS}),\ g_o = I_{DS}\lambda,\ r_o = 1/(I_{DS}\lambda)$$

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M1 5 1 3 3  MPCH_0P8 L=0.8U W=60.0U M=1
M2 6 2 3 3  MPCH_0P8 L=0.8U W=60.0U M=1
*M3 3 4 0  0 MNCH_2P0 L=2.0U W=196.0U M=1
I3 99 3 DC 180U
R3 99 3 25K
M4 5 7  0  0 MNCH_0P8 L=0.8U W=43.0U M=1
M5 6 7  0  0 MNCH_0P8 L=0.8U W=43.0U M=1
M6 8 10 5  0 MNCH_2P0 L=2.0U W=100.0U M=1
M7 9 10 6  0 MNCH_2P0 L=2.0U W=100.0U M=1
M8 8 11 12 12 MPCH_0P8 L=0.8U W=65.0U M=1
M9 9 11 13 13 MPCH_0P8 L=0.8U W=65.0U M=1
M10 12 14 99 99 MPCH_0P8 L=.8U W=65.U M=1
M11 13 14 99 99 MPCH_0P8 L=.8U W=65.U M=1
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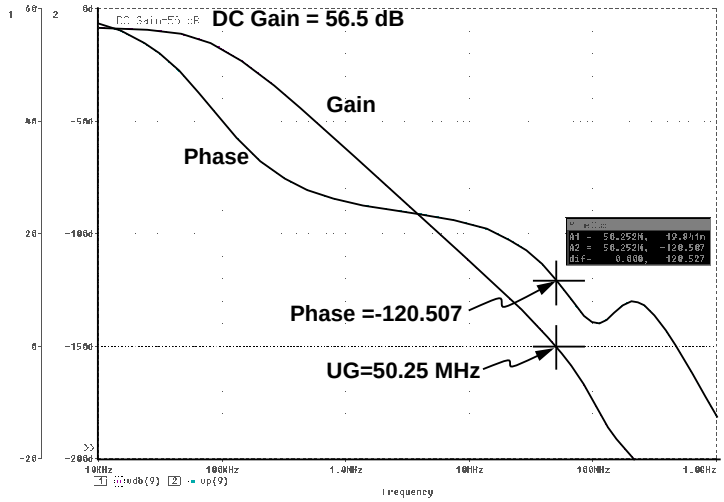
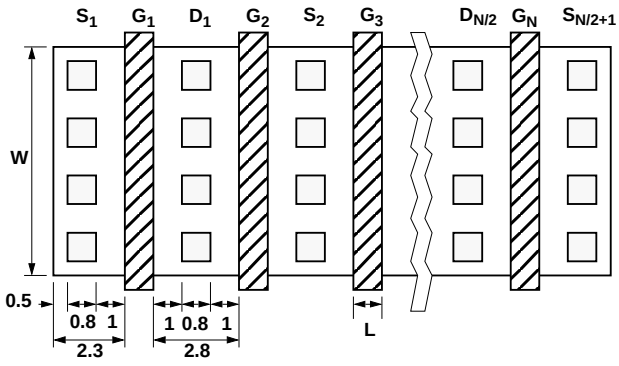
- **Note: All PMOS transistors have source tied to substrate to avoid increased threshold due to body effect. This is not possible with NMOS (since NMOS is in a common substrate) hence M6 and M7 have a slightly increased threshold. For this reason, VB3 has been raised to 1.48 V.**
- **Note also: M3 is replaced with I3 and R3 of approximately 180 uA and 25K. The value of 25K was taken from the NMOS current source from the previous example. In that case, R3 was simply 1/GDS3. It can also be calculated from from R=1/(Ixlambda). For I=200uA and lambda=0.2, R=25K. It turns out that lambda for N and P are not quite the same, so this should really be done more carefully. Mainly where this could be important is in determining common-mode gain. With the above values, the resulting current is 200 uA, if VGS1,2 =1V. It will be necessary to adjust I3 slightly when changing the size of M1 and M2, since any change of size will change the VGS, and hence the voltage across R3**
- **VFB forms the equivalent of a current mirror between M10 and M11. M10 (in series with M8) forms a diode connected transistor, that is the voltage on node 8 is directly transferred to the gate of M10 through VFB. As a result any change of current, through M10 will be mirrorred by M11. As well, being diode connected, node 8 will maintian a nearly constant voltage. Any change of voltage on this node is directly fed to the gate of M10, M11, and a small change of voltage can produce a large change of current according to $\Delta I = g_m \Delta V$. Thus as seen on the schematic, the output current is $i_{out} = g_m v_d$.**
- **Note that VFB could be turned to 0V and the circuit would still work. This particular value of VFB is very convenient, since then it is simply a straight connection. The result would be that the voltage on node 8 and node 9 would then be $V_{DD} - V_{GS10}$, which for conditions similar to before would be about 1.9V instead of 1.5 V. Thus this can be seen as an output referred offset of 0.4 V. With a DC gain of 1000, this corresponds to an input referred offset of 0.4 mV which is quite tiny. Recall that with feedback, input referred offset is typically what one would see. Thus, all one needs is a differential input of 0.4 mV and the output voltage will move by 0.4 V which will result in the output voltage being at 1.5V. Here we chose to use VFB=0.4V, so we would nominally not have any offset.**
- **The following table shows the nominal starting design, where sizes were set to result in all Vons being 0.2V and VDS for M4,M5, M10,M11 being 0.4V. Then transistor sizes were changed to attempt to achieve maximum bandwidth, which is achieved with minimum gate length. Then sizes were changed to attempt to get maximum DC gain which is obtained with larger gate lengths. Note if the design goal was to minimize offset, larger gate lengths are also important. Optimizing for low noise will be discussed later. In real life, there is usually not a single goal, but a combination of goals.**

Transistor Sizes				Transconductances, Conductances					Performance			Comments, etc	
M1,2,	M4,5	M6,7	M8-11	gm1	go1	gm67	go67	go4	Ao	UGBW	PhMrg	Limiting factor	Comments
60/0.8	43/0.8	100/2	65/0.8	598	39.6	914	21.8	69.4	42.0	41.7	82	Von=0.2	Starting Point, as on last page.
650/0.8	43/0.8	100/2	65/0.8	2050	134	919	21.9	69.4	49.7	125	61	PM=60	Larger M1,2, higher gain, BW
1000/0.8	43/0.8	16/0.8	65/0.8	2570	167	553	29.6	69.4	45.5	139	62	PM=60	All 0.8u, best UGBW
60/0.8	195/2	100/2	327/2	600	39.8	917	21.9	42.6	50.7	38.9	68	Von=0.2	M4,5 2u increases gain
120/0.8	195/2	100/2	327/2	866	56.9	915	21.8	42.6	52.4	51.8	60	PM=60	Increase M1,2 better gain
260/2	195/2	100/2	327/2	802	10.8	916	21.9	42.6	56.6	50.3	60	Von=0.2&PM=60	All transistors 2u, best gain

Plot of the last entry with largest gain



Including Transistor Parasitics. Part of real life, but not officially part of 97.477, for information only.



Transistor size is NW/L. Dimensions are W **by**

$N \times L + (N-1) \times 2.8\mu + 4.6\mu$

Area of the Source is given by

AS= $2 \times 2.3 \times W + \left(\frac{N}{2} - 1\right) \times 2.8 \times W \; = \; 1.4NW + 1.8W$

Area of Drain is AD= $\frac{N}{2} \times 2.8 \times W \; = \; 1.4NW$

Perimeter of Source is given by:

PS= $2W + 4 \times 2.3 + 2\left(\frac{N}{2} - 1\right) \times 2.8 \; = \; 2.8N + 2W + 3.6$

Perimeter of Drain is PD = $2 \times \frac{N}{2} \times 2.8 \; = \; 2.8N$

Results with parasitics included in SPICE Deck (e.g., below) with the same circuit as before. Conclusion, about 5 degrees worse phase margin, but still OK.

NW	N	W	Size	AS	AD	PS	PD
50	10	5	5x37.8	70+9=79	70	28+10+3.6=41.6	28
50	5	10	10x19.8	70+18=88	70	14+20+3.6=36.6	14
100	10	10	10x37.8	140+18=158	140	28+20+3.6=51.6	28
200	10	20	20x37.8	280+36=316	280	28+40+3.6=71.6	28
260	10	26	26x37.8	364+46.8=410.8	364	28+52+3.6=83.6	28
327	10	32.7	26x37.8	457.8+58.9=516.7	457.8	28+65.4+3.6=97.0	28
400	10	40	40x37.8	560+72=632	560	28+80+3.6=111.6	28
400	20	20	20x73.9	560+36=596	560	56+40+3.6=99.6	56

M1 5 1 3 3 MPCH_2P0 L=2.0U W=260.0U
+AD=364P AS=410P PS=84U PD=28U M=1