Department of Electronic

ELEC 5808 (ELG 6388) Signal Processing Electronics

Final Examination

Dec 13th, 2007 7:30PM - 9:30PM R. Mason

answer all questions – **TWO** 8.5 x 11 crib sheets allowed

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1. (5 points) Multiple Choice - Choose BEST Answer

(a) What is a typical input offset voltage for CMOS opamp?

- (i) 2 mV
- (ii) 2 uV
- (iii) 2 pV
- (iv) 200 mV

(b) Why do we use clocked comparators?

- (i) higher speed
- (ii) increase voltage gain
- (iii) reduce offset voltage
- (iv) increase input impedance

(c) Which DAC specification would determine accuracy?

- (i) sampling rate
- (ii) sampling jitter
- (iii) gain error
- (iv) effective number of bits

(d) You can reduce the input referred white noise of a basic single stage opamp by:

- (i) reducing the supply current
- (ii) reducing the diff pair transistor lengths
- (iii) using p-channel diff pair transistors
- (iv) lowering the supply voltage

(e) Which of the following could be used to improve the accuracy of a basic MOS sample and hold circuit?

- (i) reduce the sampling capacitor size
- (ii) use a single ended configuration
- (iii) increase the sampling transistor size
- (iv) increase the output buffer input capacitance

2. (20 points) Short Answer

(a) In the basic two stage opamp, is it better to have the first stage differential pair implemented with NMOS or PMOS transistors? Why?

(b) Given an ideal 10 bit ADC which would have a larger SNR a $1V_{RMS}$ sinusoid or a $1V_{RMS}$ random signal? Why?

(c) Draw an example of a common mode feedback circuit (transistor level) and explain how it works.

(d) How can we reduce charge injection in clocked comparators?

(e) Why do we use a preamp in a track and latch comparator? Draw a circuit diagram of a simple track and latch comparator and identify the preamp and latch stages.

(f) Why do we use wide swing current mirrors? What is their disadvantage? Draw a circuit diagram of a simple wide swing current mirror.

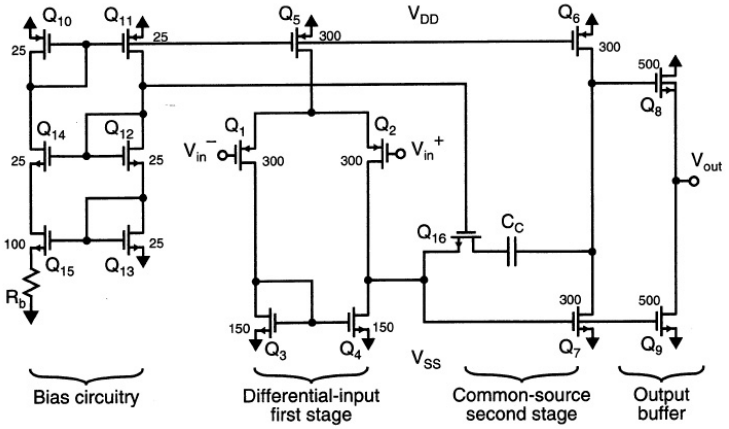
(g) What is 1/f noise and how can we reduce it in CMOS circuits?

(h) Why do we tend not to use minimum channel length transistors in analog circuits? When would you use minimum channel length transistors in analog circuits?

(i) Why do we use 2's complement arithmetic in many bipolar (i.e. positive and negative inputs) converters?

(j) Which tends to have better DNL a thermometer coded, binary weighted or R-2R DAC? Why?

3. (5 points) Given the following opamp circuit and transistor parameters. Assume I_{D5} = 100 uA, all transistor lengths are 1.2 μm, and C_C = 10 pF. (a) estimate the -3dB frequency of the first stage, (b) estimate the unity gain frequency of the opamp, (c) find the slew rate.



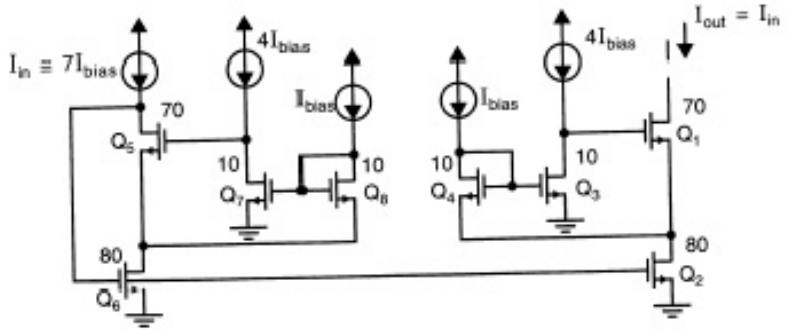
n-channel MOS transistors:

$\mu_n C_{ox} = 92\ \mu A/V^2$
$V_{tn} = 0.8\ V$
$\gamma = 0.5\ V^{1/2}$
$r_{ds}(\Omega) = 8{,}000\ L(\mu m)/I_D(mA)$ in active region
$C_j = 2.4 \times 10^{-4}\ pF/(\mu m)^2$
$C_{j\text{-}sw} = 2.0 \times 10^{-4}\ pF/\mu m$
$C_{ox} = 1.9 \times 10^{-3}\ pF/(\mu m)^2$
$C_{gs(overlap)} = C_{gd(overlap)} = 2.0 \times 10^{-4}\ pF/\mu m$

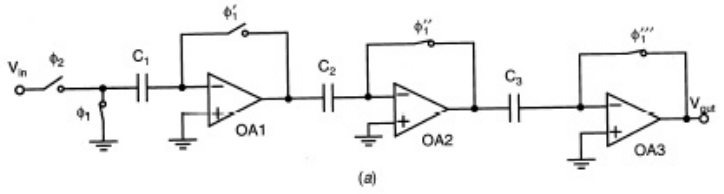
p-channel MOS transistors:

$\mu_p C_{ox} = 30\ \mu A/V^2$
$V_{tp} = -0.9\ V$
$\gamma = 0.8\ V^{1/2}$
$r_{ds}(\Omega) = 12{,}000\ L(\mu m)/I_D(mA)$ in active region,
$C_j = 4.5 \times 10^{-4}\ pF/(\mu m)^2$
$C_{j\text{-}sw} = 2.5 \times 10^{-4}\ pF/\mu m$
$C_{ox} = 1.9 \times 10^{-3}\ pF/(\mu m)^2$
$C_{gs(overlap)} = C_{gd(overlap)} = 2.0 \times 10^{-4}\ pF/\mu m$

4. (5 points) Explain the purpose of each component in the circuit below.



5. (5 points) For the circuit below. (a) Find the voltages at each of the opamp inputs at the end of ϕ_1', ϕ_1", ϕ_1"', ϕ_1, and ϕ_2 where V_i is the input and $V_{err\text{-}i}$ is the error due to the reset switch of the ith opamp. Assume opamps are offset free and that they remain in their linear region after the reset switch is opended. (b) Explain how this circuit minimizes charge injection errors.



(a)