**ENEL5808** **Student Name** _____
**Signal Processing Electronics**
**Mid-Term Examination** **Student Number** _____

Oct. 22,2009 7:30PM - 9:00PM R. Mason
answer all questions on sheet provided

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1. (5 points) Multiple Choice, Circle BEST answer

(a) Which of the following would **NOT** require a mask in a CMOS process:
- (i) contact
- (ii) pplus
- (iii) substrate
- (iv) polysilicon

(b) A resistor has length = 20um, width = 10um, height = 0.5um and sheet resistance of 20 ohms/square. What is the total resistance:
- (i) 10 ohms
- (ii) 20 ohms
- (iii) 40 ohms
- (iv) 80 ohms

(c) How do noise sources added up in a circuit:
- (i) root of the sums
- (ii) sum of the squares
- (iii) square of the sums
- (iv) sum of the inverses

(d) The Miller capacitance of a common source amplifier is dominated by:
- (i) $C_{gs}$
- (ii) $C_{gd}$
- (iii) $C_{ds}$
- (iv) $C_{ox}$

(e) Which of the following is **NOT** a typical layout rule:
- (i) minimum spacing of a layer
- (ii) minimum height of a layer
- (iii) minimum dimension of a layer
- (iv) minimum overlap of another layer

2. (10 points) Short Answer

(a) Draw the low frequency small signal model of a basic NMOS current mirror. Show all resistors and transconductors.

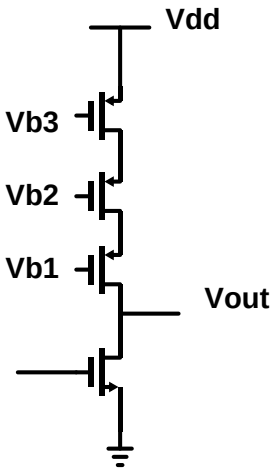
(b) Give three examples of layout design rules that you followed for the 0.18 μm CMOS tristate driver layout you did.

(c) What is the body effect? Is it normally good or bad? Why?

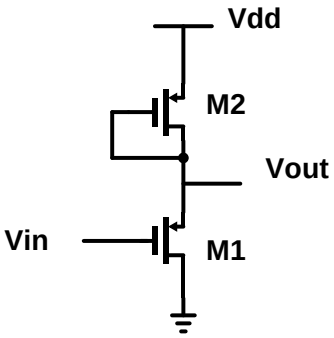
(d) A resistor and capacitor are connected in parallel. The resistor is 1Kohm and the capacitor is 1pF. What is the RMS noise voltage across the capacitor (assume: k = 1.38 x $10^{-23}$ J/K and T = 300K )

(e) Draw the schematic for a telescopic differential PMOS cascode gain stage with NMOS casocde loads and a PMOS current mirror for generating the differential pair bias current. What is the output impedance of this amplifier?

3. (5 points) For the following circuit assuming all transistors are in saturation and have W/L = 100um/1.5um, $u_nC_{ox}$ = 80 uA/V², $u_pC_{ox}$ = 40uA/V² , $I_D$ = 100uA, $r_{ds\text{-}n}$ (ohms) = $r_{ds\text{-}p}$ (ohms) = 6,000L (um)/$I_d$ (mA), Ignoring the body effect, what is the gain of this stage?

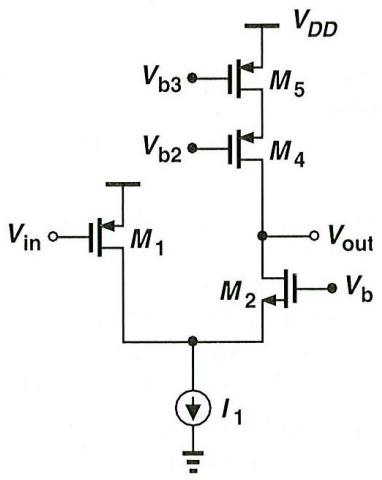



4. (4 points) Draw and label the DC transfer function (Vout vs. Vin) for the following circuit. Explain the purpose of M1 and M2. What kind of circuit is this normally referred to as?



5. (6 points) What are the following circuits? Explain the purpose of each transistor in the circuits.

(a)




(b)