Department of Electronic

ELEC 5808 (ELG 6388) Signal Processing Electronics

Final Examination

Dec 14th, 2010 5:30PM - 7:30PM R. Mason

answer all questions – one 8.5 x 11 crib sheets allowed

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1. (5 points) Multiple Choice - Choose **BEST** Answer

(a) The difference between opamp output phase and -180^{O} at unity gain is called?

- (i) gain margin
- (ii) unity gain phase difference
- (iii) phase margin
- (iv) unity gain crossover frequency

(b) Latched comparators are usually very fast because they?

- (i) have large open loop gain
- (ii) have positive feedback
- (iii) have low paracitic resistance
- (iv) have diode connected transistors

(c) What is the typical voltage gain of the basic two stage CMOS opamp we studied?

- (i) 20dB
- (ii) 40dB
- (iii) 80dB
- (iv) 100dB

(d) For the basic two stage CMOS opamp why do we use a transistor for lead compensation

- (i) lower power consumption
- (ii) better matching
- (iii) less noise
- (iv) fewer connections

(e) Which of the following could be used to improve the accuracy of a basic MOS sample and hold circuit?

- (v) reduce the sampling capacitor size
- (vi) use a single ended configuration
- (vii) increase the sampling transistor size
- (viii) increase the output buffer input capacitance

2. (20 points) Short Answer

(a) In the basic two stage opamp, is it better to have the first stage differential pair implemented with NMOS or PMOS transistors? Why?

(b) Why would you use a single stage folded cascode opamp instead of the basic two stage CMOS opamp you studied?

(c) When and Why do we need a common mode feedback circuit? Draw a (transistor level) common mode feedback circuit.

(d) Why is usually important to make the sampling clock rise/fall time small in a sample and hold circuit?

(e) Why do we use a preamp in a track and latch comparator? Draw a circuit diagram of a simple track and latch comparator and identify the preamp and latch stages.

(f) Why do we use wide swing current mirrors? What is their advantage? Draw a circuit diagram of a simple wide swing current mirror.

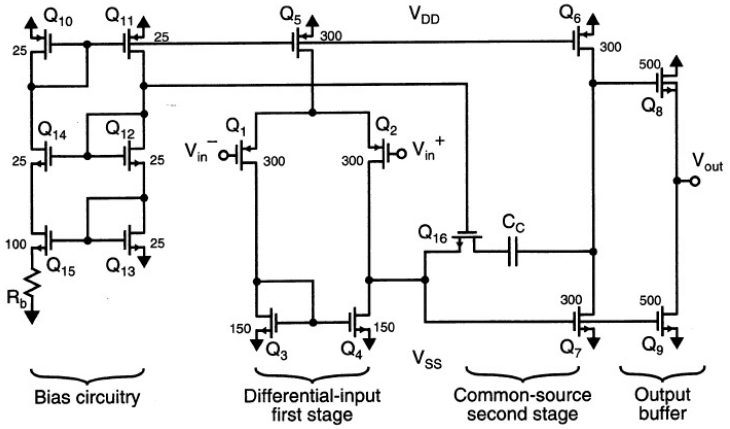
(g) What is 1/*f* noise and how can we reduce it in CMOS circuits?

(h) Why do we tend not to use minimum channel length transistors in analog circuits? When would you use minimum channel length transistors in analog circuits?

(i) What is the purpose of the compensation capacitor C_C in the basic two stage opamp?

(j) How can we reduce charge injection in clocked comparators?

3. (5 points) Given the following opamp circuit and transistor parameters. Ignoring the body effect, assume I_{D5} = 100 uA, all transistor lengths are 1.6 μm, +/- 5V power supplies and C_C = 10 pF. (a) what is the output voltage range of the opamp, (b) estimate the range of the common mode input voltage.



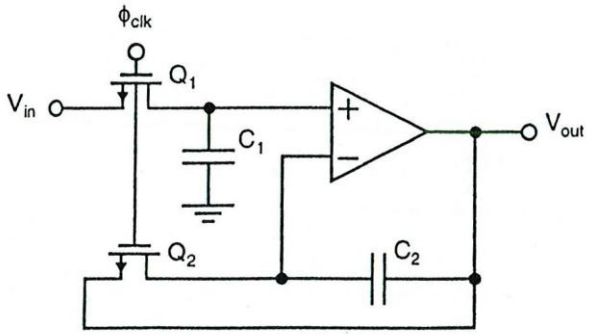
n-channel MOS transistors:

$\mu_n C_{ox} = 92\ \mu A/V^2$
$V_{tn} = 0.8\ V$
$\gamma = 0.5\ V^{1/2}$
$r_{ds}(\Omega) = 8{,}000\ L(\mu m)/I_D(mA)$ in active region
$C_j = 2.4 \times 10^{-4}\ pF/(\mu m)^2$
$C_{j\text{-}sw} = 2.0 \times 10^{-4}\ pF/\mu m$
$C_{ox} = 1.9 \times 10^{-3}\ pF/(\mu m)^2$
$C_{gs(overlap)} = C_{gd(overlap)} = 2.0 \times 10^{-4}\ pF/\mu m$

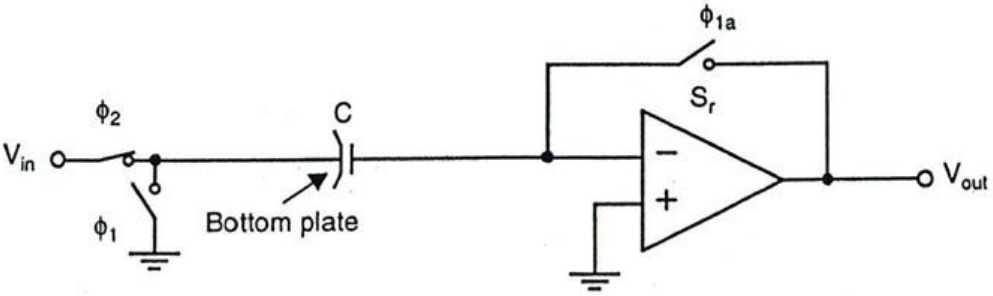
p-channel MOS transistors:

$\mu_p C_{ox} = 30\ \mu A/V^2$
$V_{tp} = -0.9\ V$
$\gamma = 0.8\ V^{1/2}$
$r_{ds}(\Omega) = 12{,}000\ L(\mu m)/I_D(mA)$ in active region,
$C_j = 4.5 \times 10^{-4}\ pF/(\mu m)^2$
$C_{j\text{-}sw} = 2.5 \times 10^{-4}\ pF/\mu m$
$C_{ox} = 1.9 \times 10^{-3}\ pF/(\mu m)^2$
$C_{gs(overlap)} = C_{gd(overlap)} = 2.0 \times 10^{-4}\ pF/\mu m$

4. (5 points) What is this circuit? Explain the purpose of each component in the circuit.



5. (5 points) For the circuit below. (a) What type of circuit is this? (b) Explain how it can elliminate the input offset voltage of the opamp (c) What effect does the opamp 1/*f* noise have on this circuit?



6. (5 points) For the circuit shown below, determine the low-frequency small-signal output vo as a function of v1,v2, the MOSFET transconductance g_m, R, and the MOSFET drain-source resistance r_{ds}. Assume all devices are in saturation. Assume r_{ds} is the same for all MOSFETs. Assume g_m is the same for all MOSFETs.