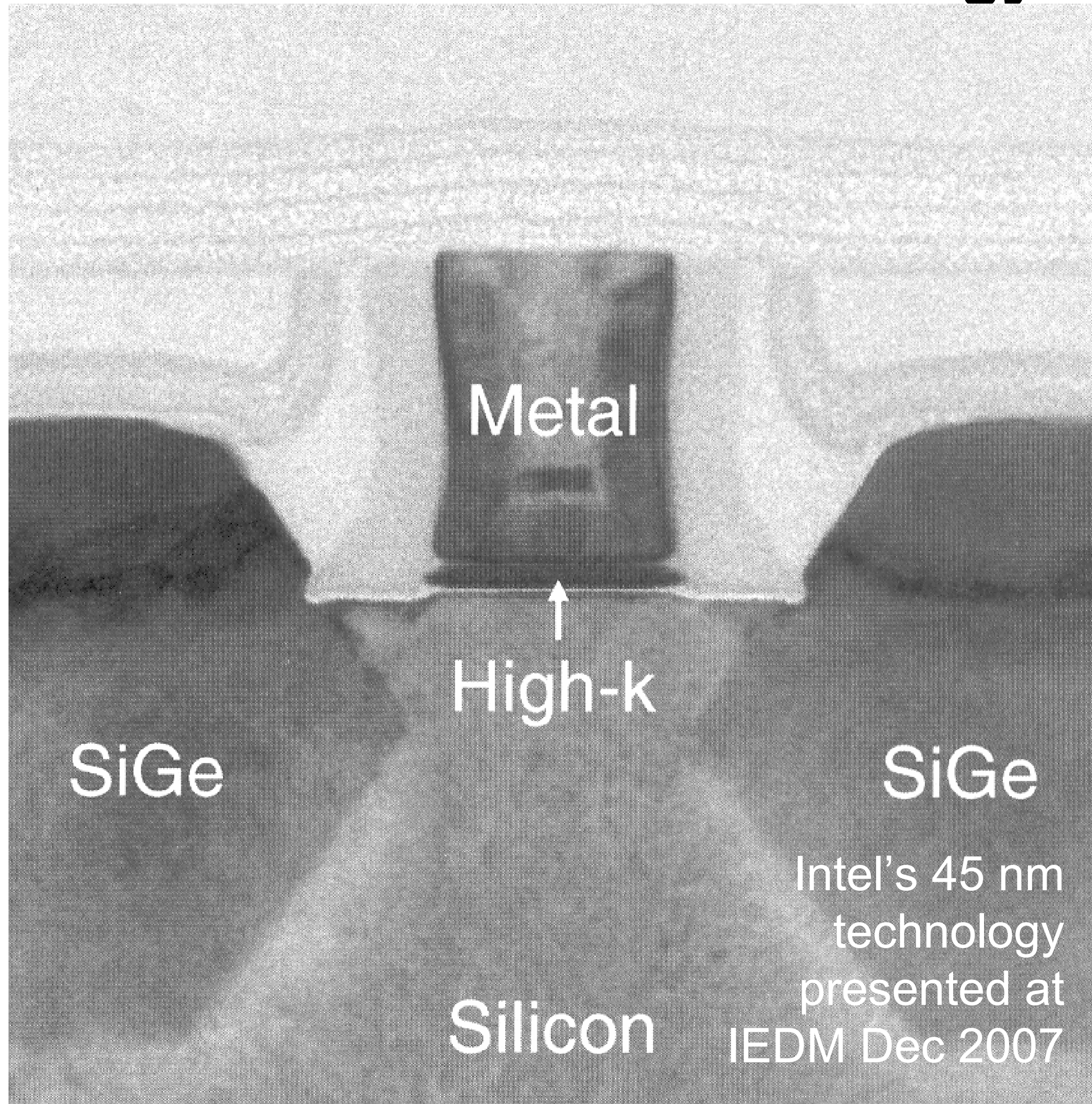
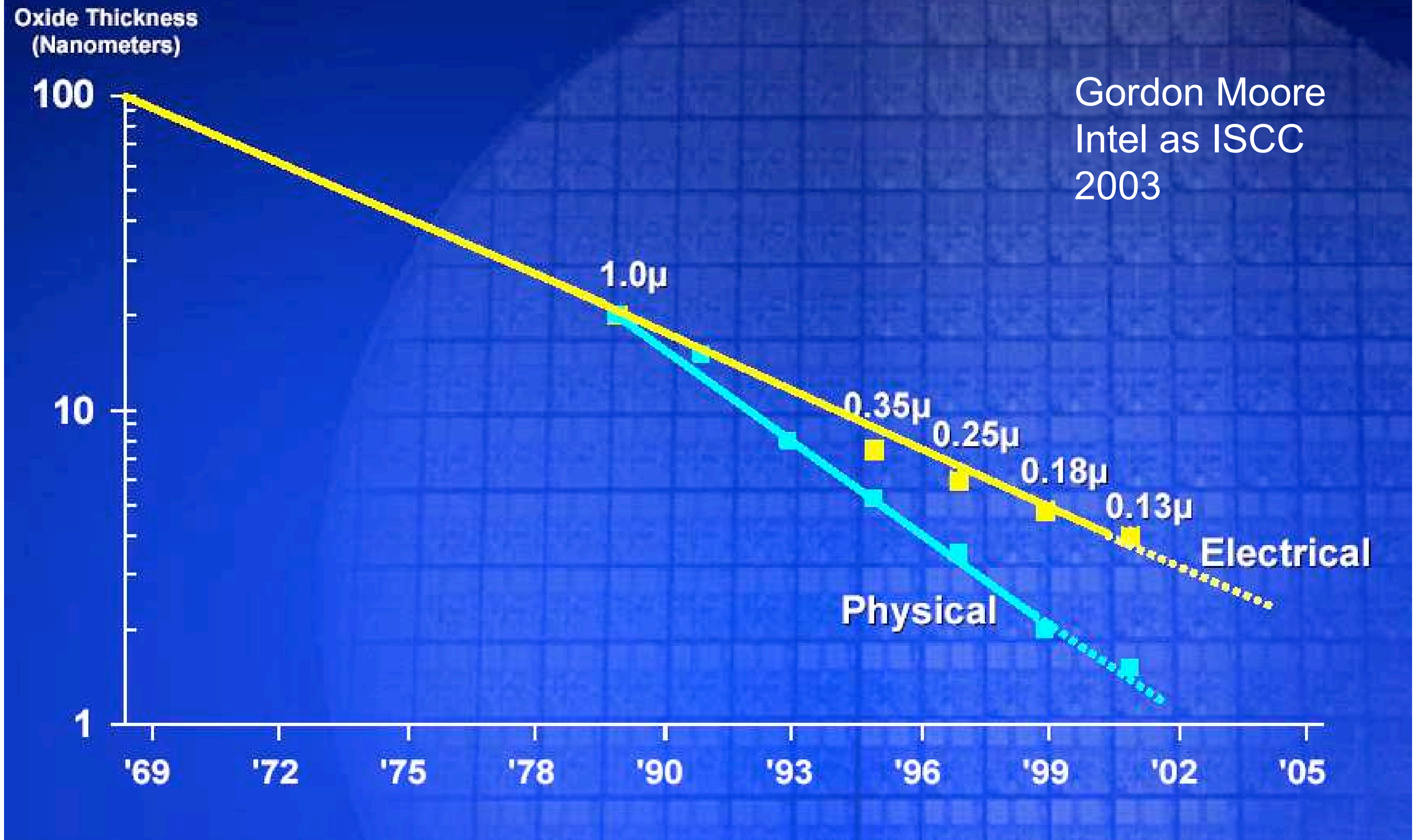
Advanced MOSFET Technology



Thin Gate Oxides (insulators)

- Gate Capacitance Attenuation- doesn't scale with oxide thickness
  - Quantum confinement in inversion channel
  - Depletion of poly gate
- Tunneling current (leakage)
  - Maximum allowable gate current sets minimum physical thickness
  - High k materials/sandwiches
- Interface atom counting
  - Fundamental limit for SiO_2 thickness


Minimum Insulator Thickness vs Time
Oxide Thickness
(Nanometers)
100
10
1
'69
'72
'75
'78
'90
'93
'96
'99
'02
'05
1.0μ
0.35μ
0.25μ
0.18μ
0.13μ
Electrical
Physical
Gordon Moore
Intel as ISCC
2003

IEEE ELECTRON DEVICE LETTERS, VOL. 17, NO. 11, NOVEMBER 1996 521

Gate Capacitance Attenuation in MOS Devices with Thin Gate Dielectrics

K. S. Krisch, *Member, IEEE*, J. D. Bude, *Member, IEEE*, and L. Manchanda, *Member, IEEE*

- Observations below 10 nm oxide thickness –
  - Oxide measured to be 5 nm physical thickness acts like 6 nm
- Modeling
  - F-D degenerate carrier statistics
  - Q-M confinement in inversion channel
  - Depletion in poly gate
- Experiments
  - High Frequency and Quasi-static C-V
  - 4.2 x 10^{-4} cm^2 capacitor area
  - Gates doped with P $5\times10^{15}/cm^2$ 160 nm thick poly
  - 3×10^{20} P/cm^3, measured 7×10^{19} $carriers/cm^3$, simulated 4×10^{19} $/cm^3$

Quantum confinement in the inversion layer

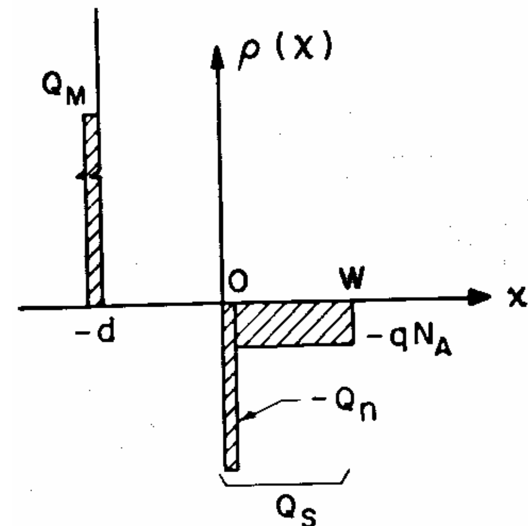
- DeBroglie wavelength of an electron in the channel:

$$E = \frac{3}{2}kT \approx 0.04eV$$

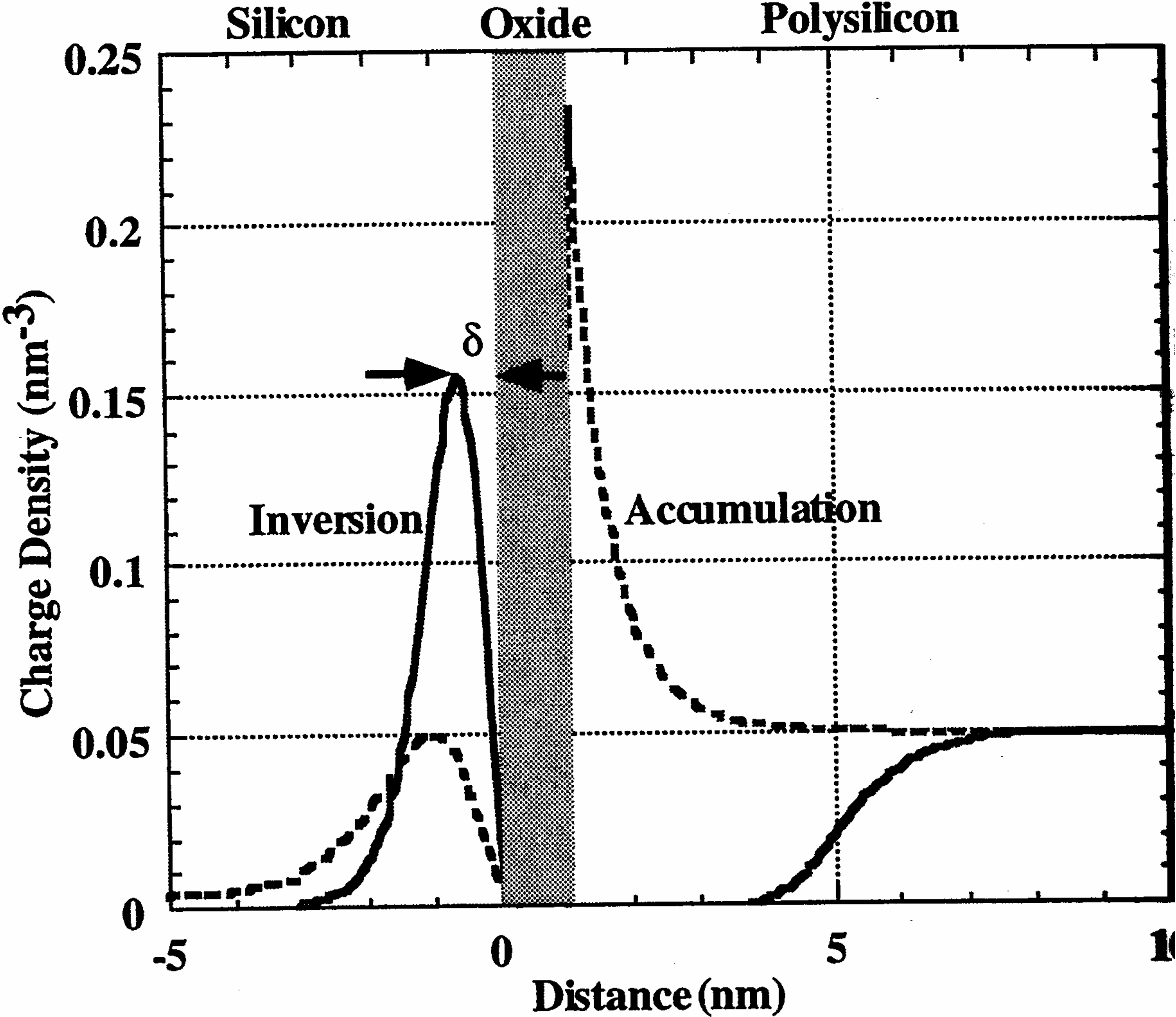
$$\lambda = \frac{h}{p} = \frac{h}{\sqrt{2mE}} \approx 6nm$$

- Thickness of inversion channel:
  - For Si x~3 nm
- Quantum confinement
  - particle in a box
- Solve self-consistent Schrodinger and Laplace equations

$\Rightarrow$ Peak of probability distribution *not* at the surface



Confinement-depletion picture



Carrier concentrations

- number of electrons in conduction band

$$n = \int_{E_c}^{E_{top}} g_c(E) f(E) dE$$

- number of holes in valence band

$$p = \int_{E_{bottom}}^{E_v} g_v(E)\left[1 - f(E)\right] dE$$

- Where:

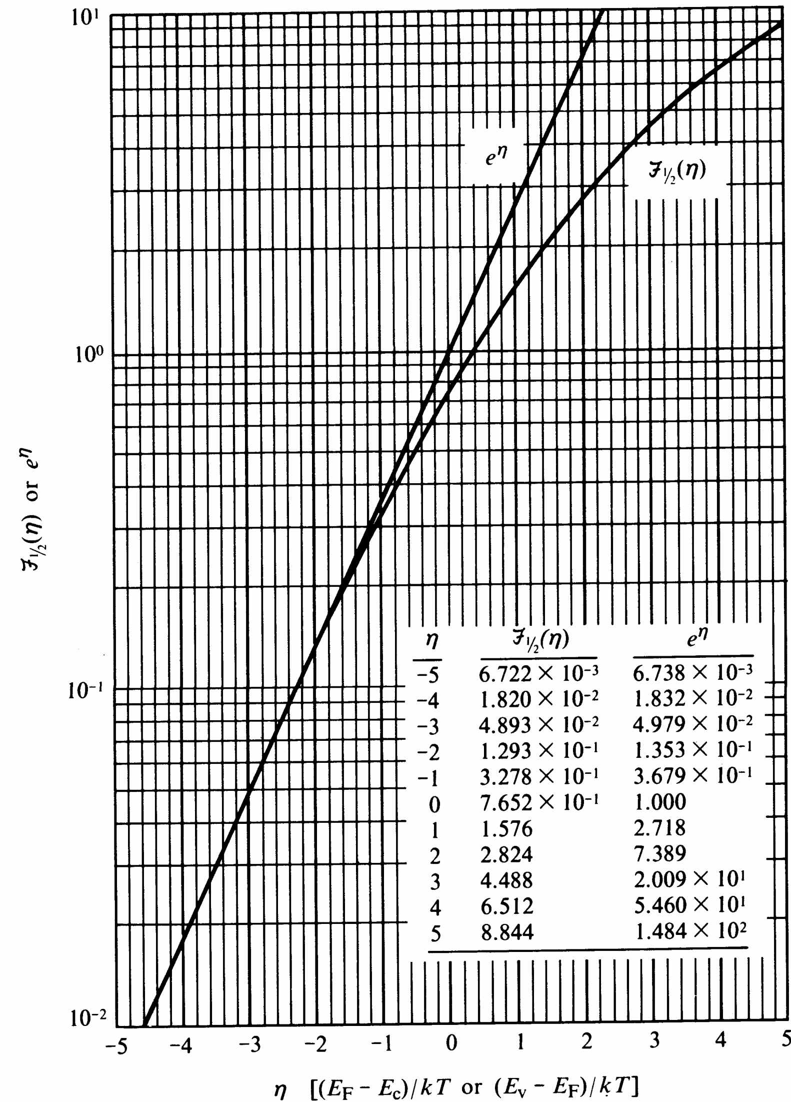
$$f(E) = \frac{1}{1 + e^{(E - E_F)/kT}}$$

Full F-D statistics

$$n = N_C \frac{2}{\sqrt{\pi}} F_{1/2}(\eta_c)$$

$$F_{1/2}(\eta) = \int_0^{\infty} \frac{\xi^{1/2} d\xi}{1 + e^{\xi - \eta}}$$

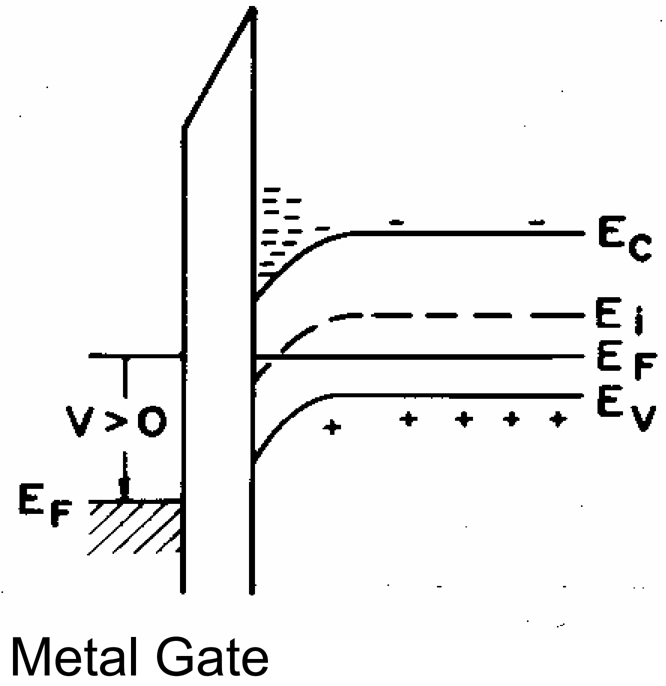
$$\eta_c = (E_F - E_C)/kT$$



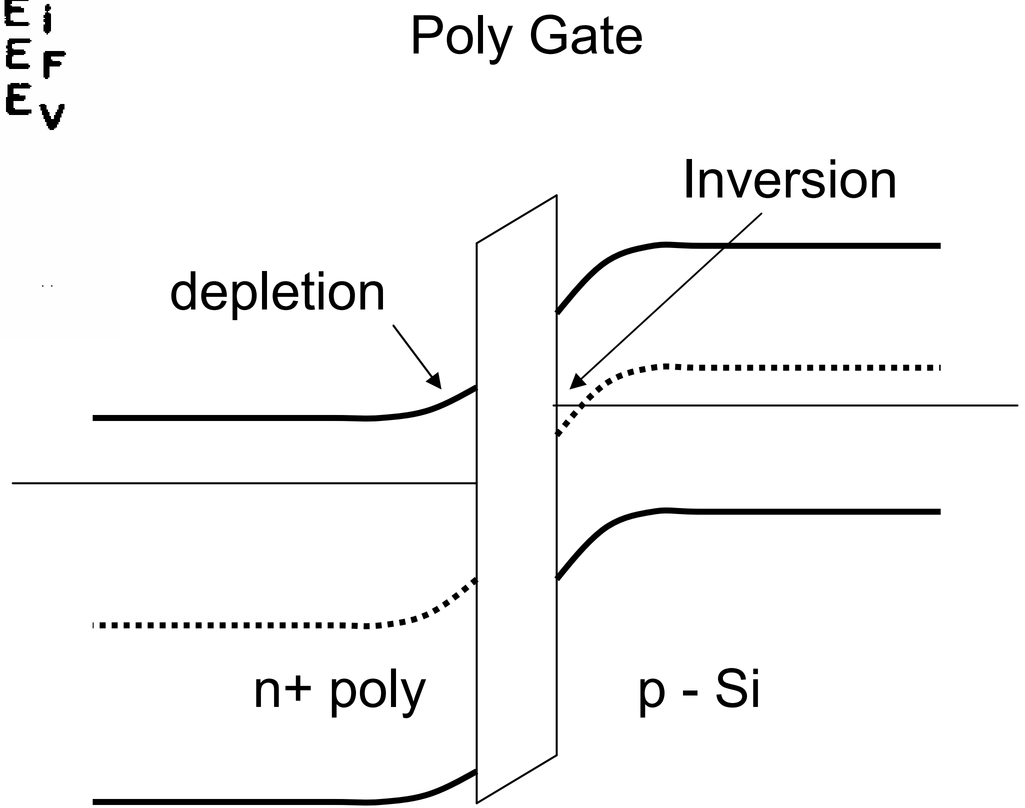
η	$\mathcal{F}_{1/2}(\eta)$	e^{η}
−5	6.722×10^{-3}	6.738×10^{-3}
−4	1.820×10^{-2}	1.832×10^{-2}
−3	4.893×10^{-2}	4.979×10^{-2}
−2	1.293×10^{-1}	1.353×10^{-1}
−1	3.278×10^{-1}	3.679×10^{-1}
0	7.652×10^{-1}	1.000
1	1.576	2.718
2	2.824	7.389
3	4.488	2.009×10^{1}
4	6.512	5.460×10^{1}
5	8.844	1.484×10^{2}

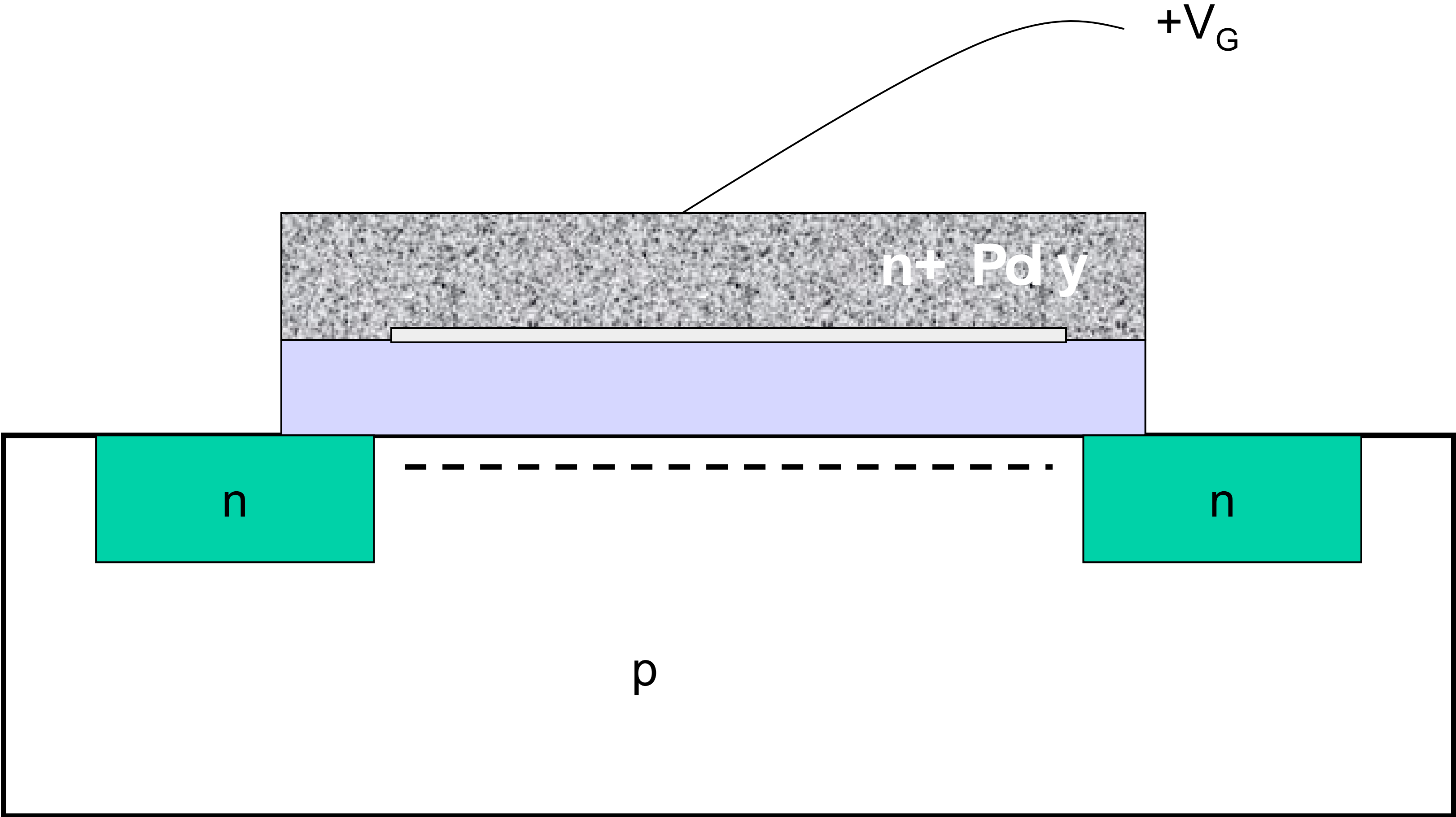
Poly Gate Depletion

- Heavily doped polysilicon does not act like a metal
- Doping activation is seen to be less at poly-oxide interface
- Depletion region can be formed at poly-oxide interface when channel is inverted
- Thickness of depletion depends on doping and applied voltage
- Higher applied voltage results in larger depletion width and decrease in overall capacitance
- C-V curves will have a downward slope
- Better Activation, Metal Gates?



Metal Gate

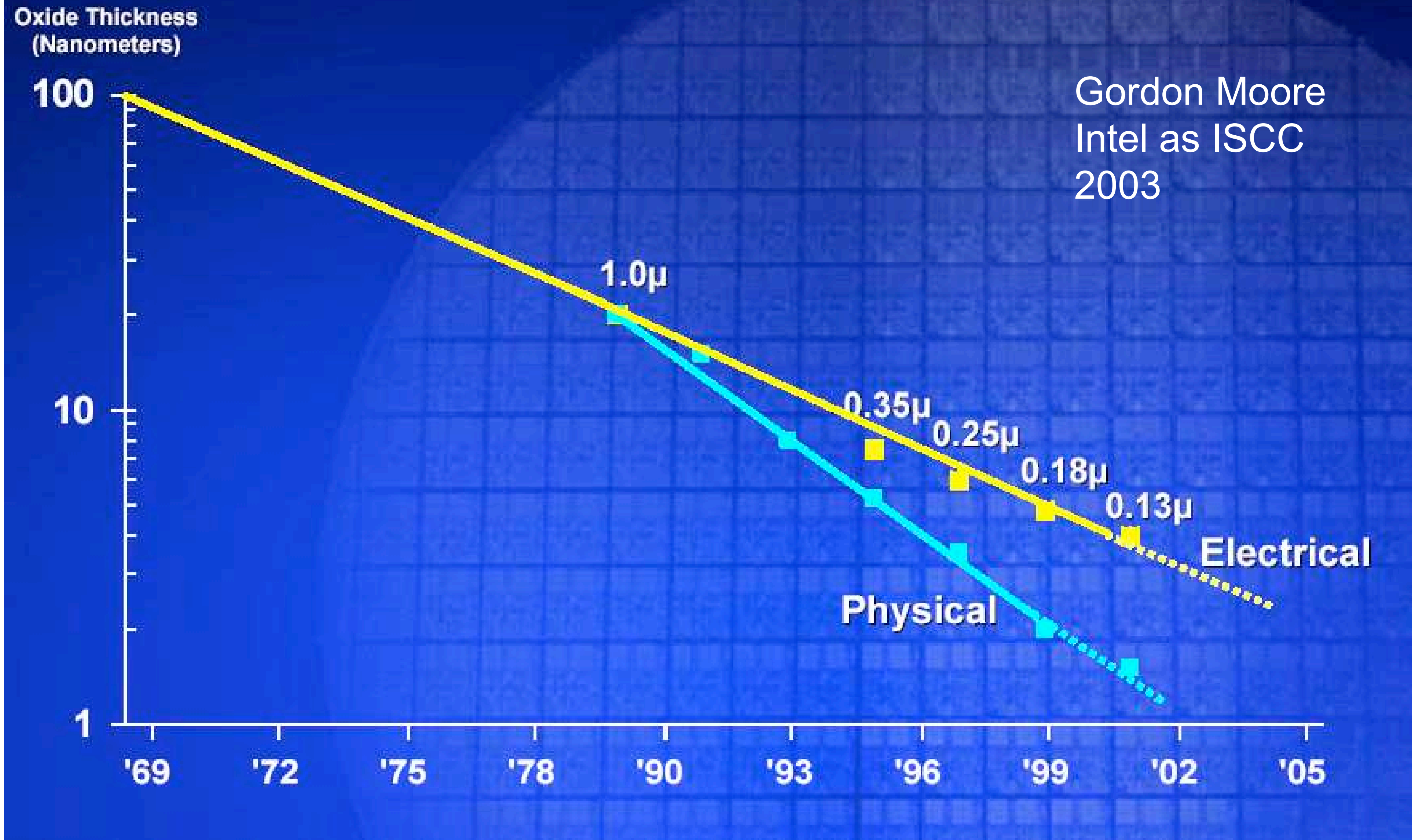




+V_G
n+ Pd y
n
n
p

Summary of Gate Capacitance Attenuation Paper

- Reduced capacitance observed for d<10 nm
- Calculations done including three effects
  - F-D statistics for carriers
  - QM confinement in channel
  - Depletion in polysilicon
- Results match well to experimental CV curves
- Simple chart calculated showing apparent gate insulator thickness as a function of measured physical oxide thickness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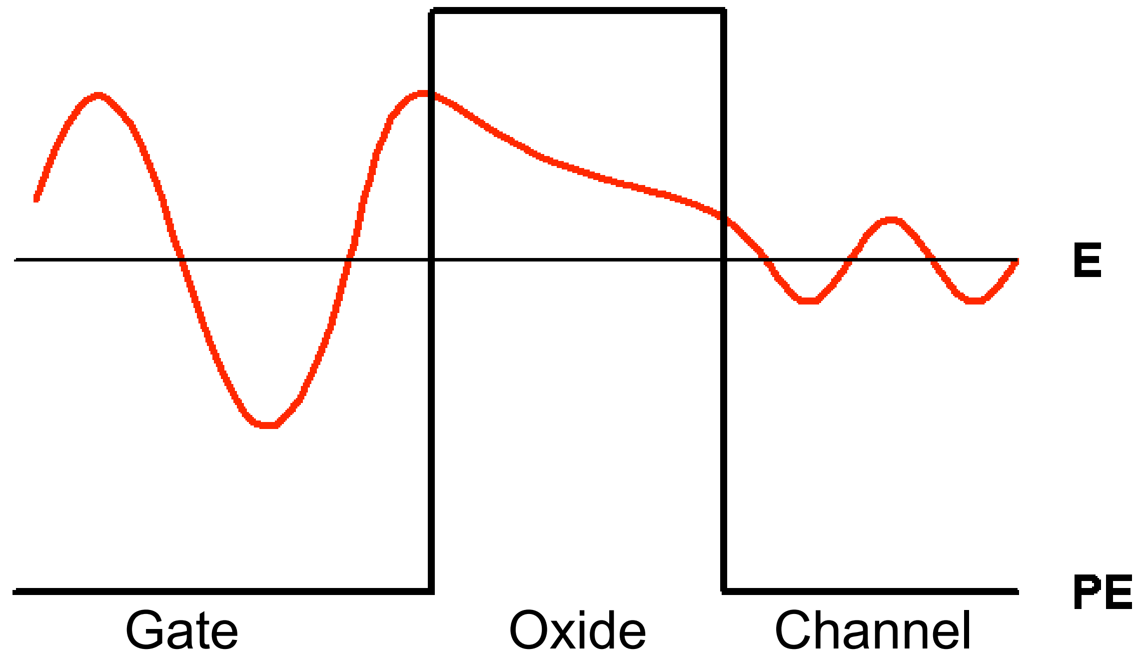
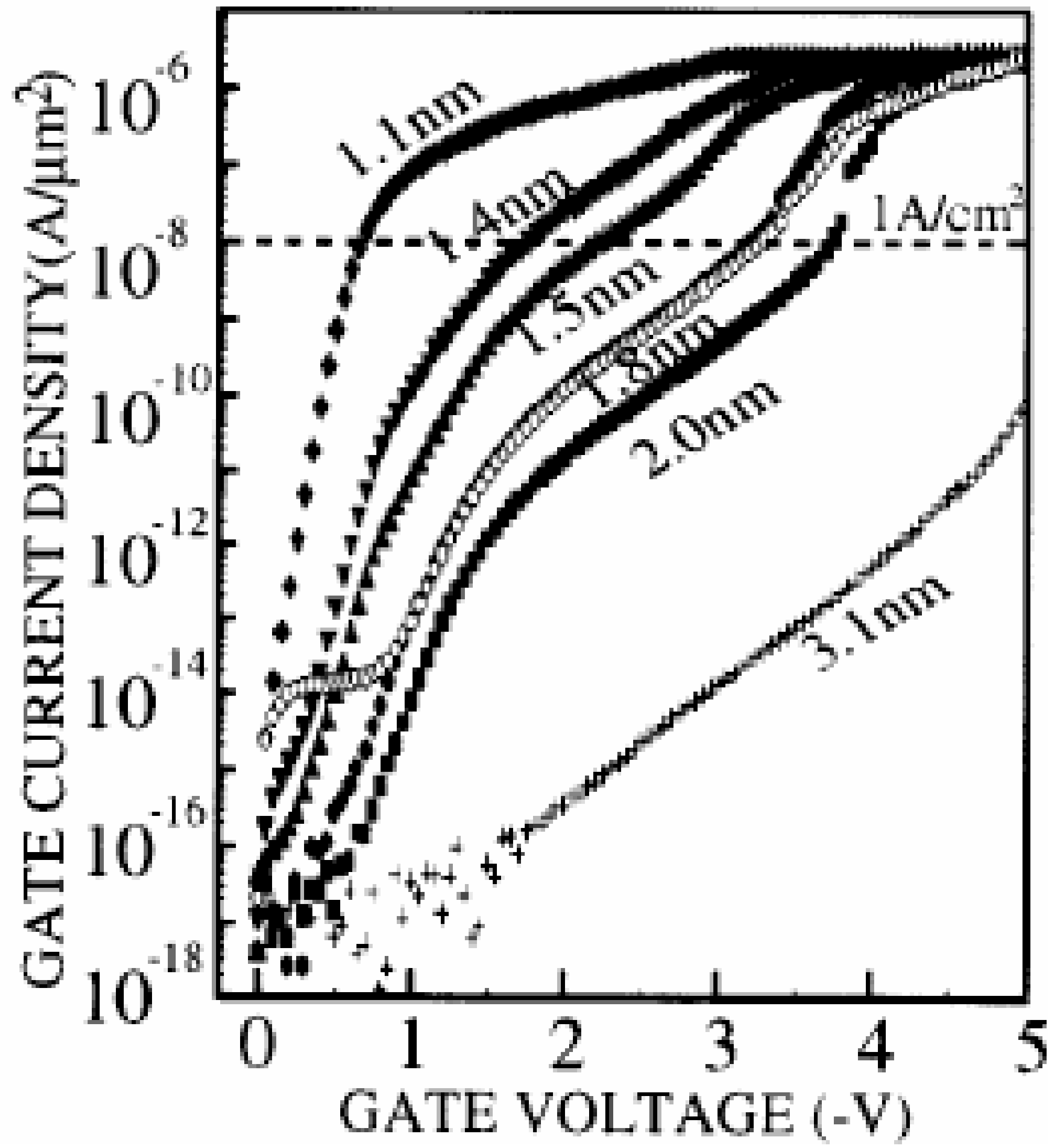
Electrical
Physical
Gordon Moore
Intel as ISCC
2003

Tunneling

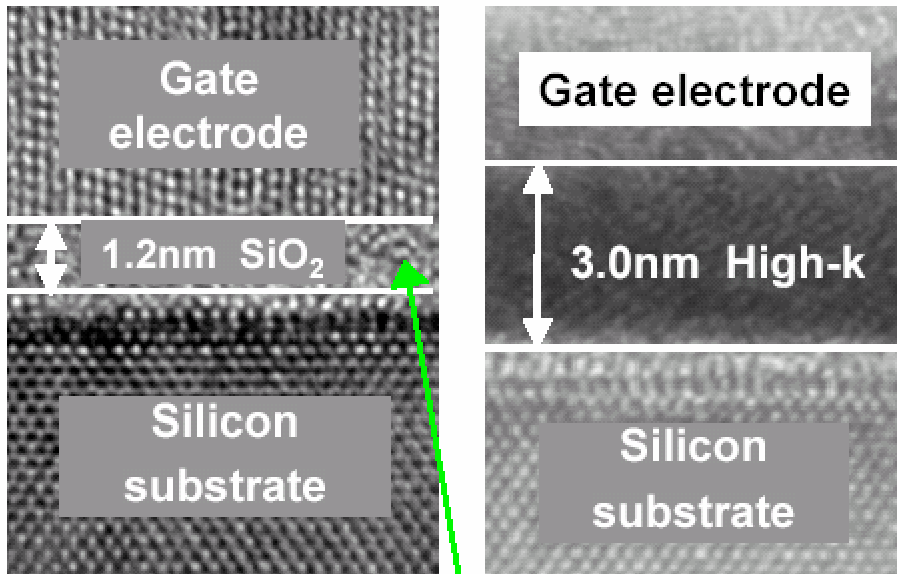


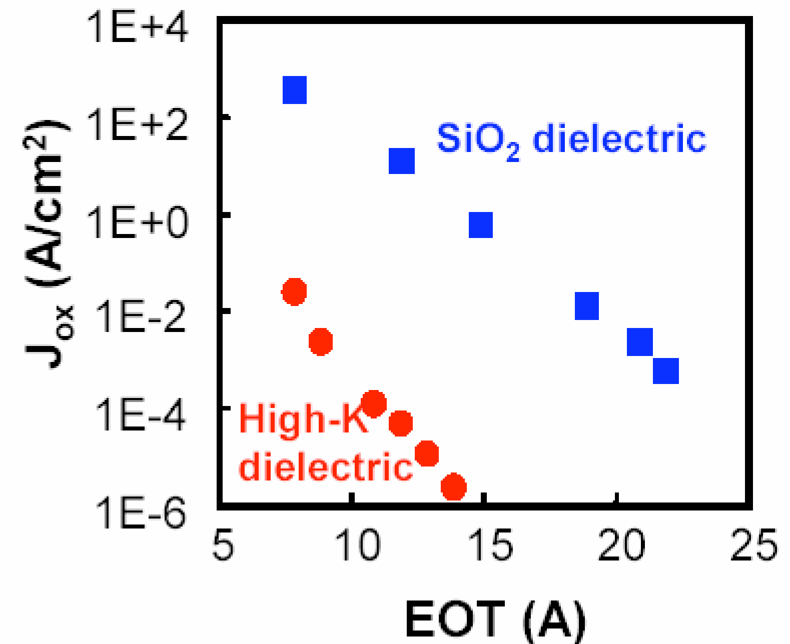
For thin barriers, finite probability of "tunneling" through
Probability of finding particle $\sim\Psi^2$
Depends on barrier height and thickness – exponentially
Gate capacitor will conduct with tunneling current



B. Weir et. al.

New Nanotechnology (e.g. ALD) to Craft New Material (e.g. High-K Gate Dielectrics)





90 nm node (in production)

	SiO2	High-k
Capacitance:	1.0x	1.6x
Leakage:	1.0x	< 0.01x

M. Radosavljevic and R. Chau, Intel Corporation

DARPA CMOS–Nano, 01/12/04

Processor Power (Watts) - Active & Leakage

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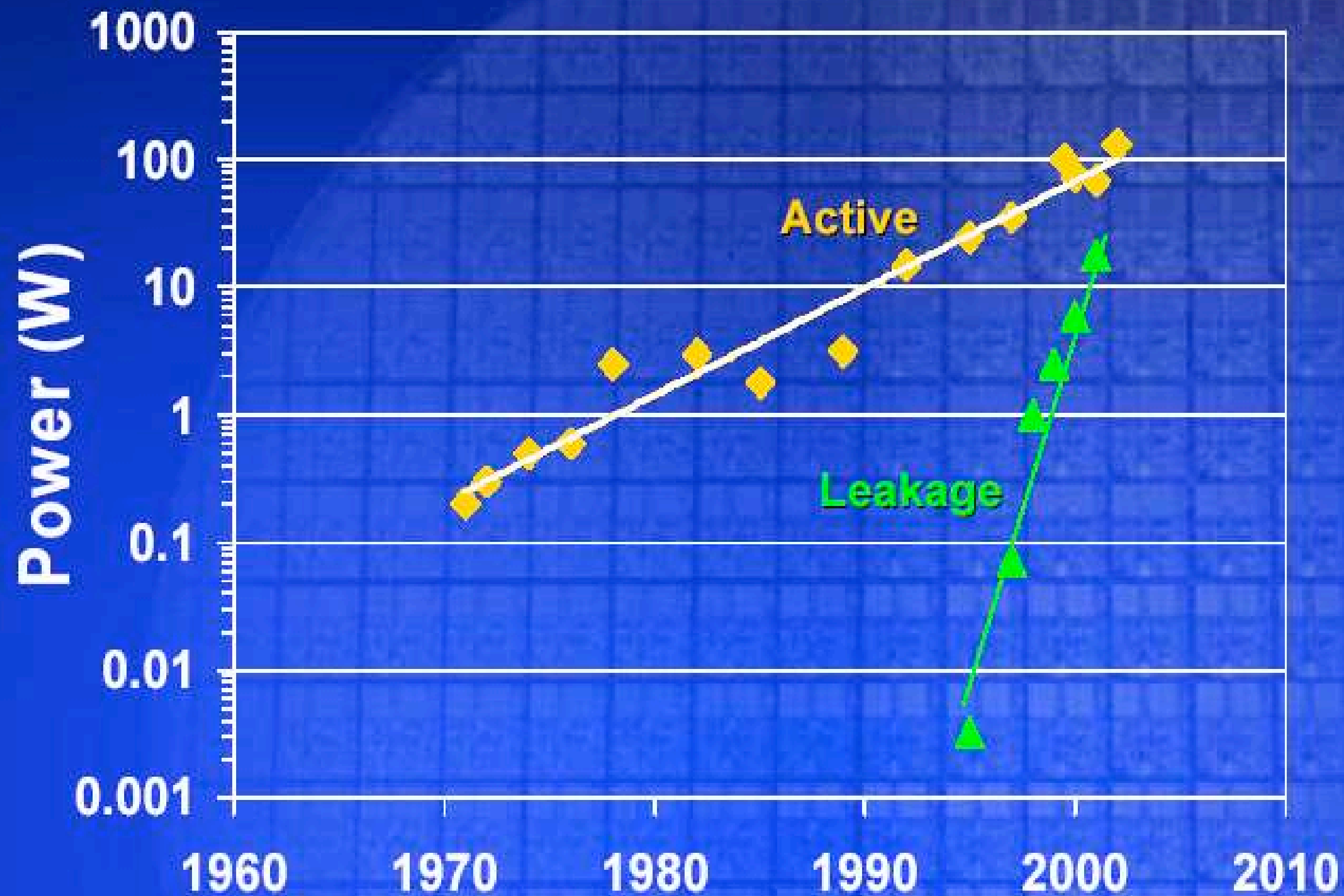
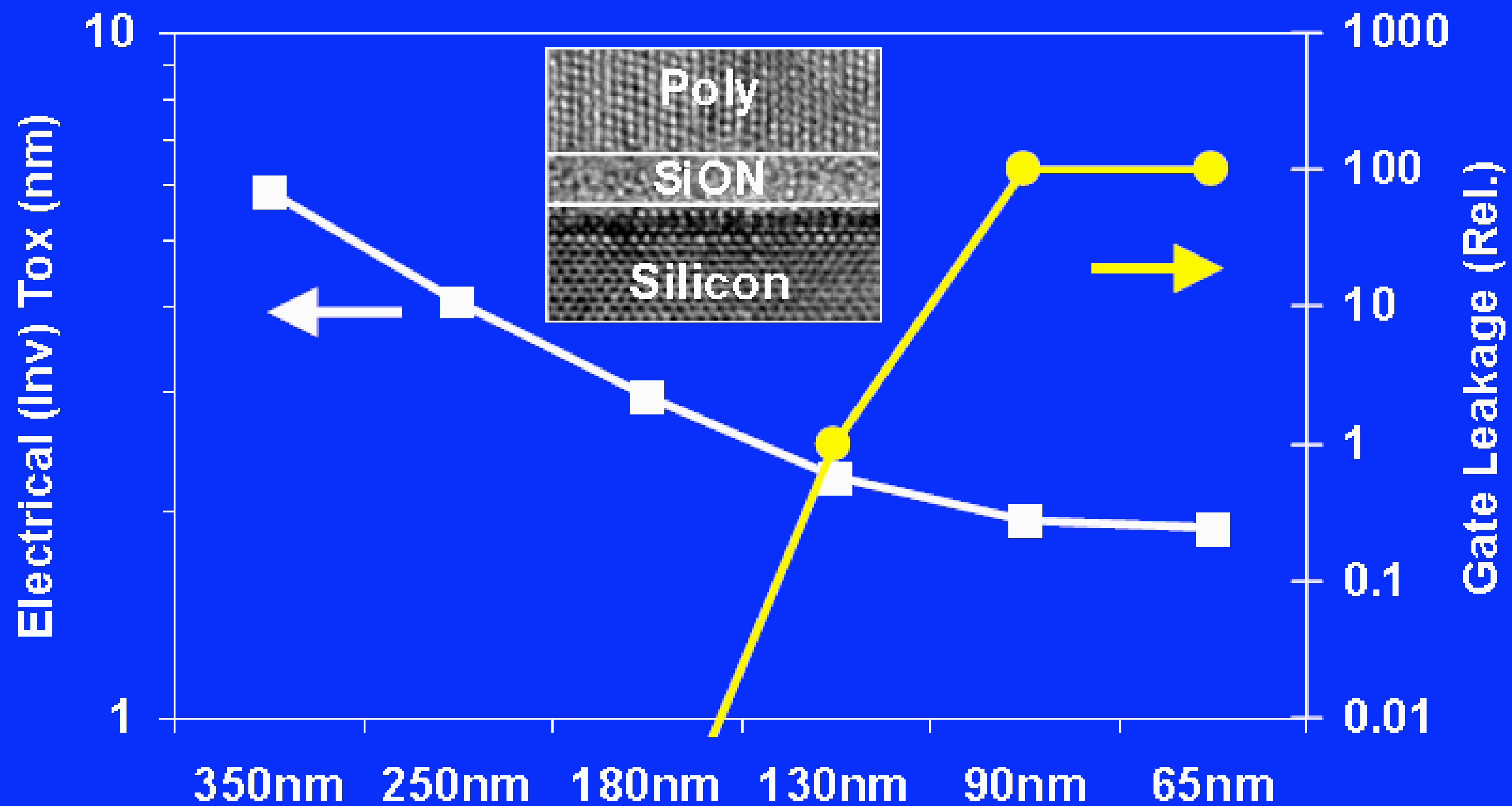


Introduction

- SiON scaling running out of atoms
- Poly depletion limits inversion T_{OX} scaling



Intel at IEDM Dec 2007

Gate Insulator Limits

- Gate capacitors act thicker than they really are due to QM confinement and poly gate depletion – heavier doping –metal gates help
- Tunneling current will limit oxide thickness to >1 nm from leakage current considerations
- Fundamental oxide thickness limit set by 2 atoms of interfacial oxide + tunneling barrier + roughness =~1-1.2 nm
- Adding higher k dielectrics in stacks doesn’t help much
- Other materials? Interface state density? Leakage?
- Other structures?

High-k + Metal Gate Benefits

- High-k gate dielectric
  - Reduced gate leakage
  - T_{OX} scaling
- Metal gates
  - Eliminate polysilicon depletion
  - Resolves V_T pinning and poor mobility for high-k dielectrics

Strained Silicon

- Biaxial or Uniaxial stress can improve mobility and transistor performance
- Stress can be introduced with
  - lattice mismatch of Si-Ge in the channel or Source/Drain
  - Deposited films with high stress
- Stress can be compressive or tensile
  - Both electron and hole mobility must be improved
  - Intel Process
    - Compression for pmos –Si-Ge S/D
    - Tension for nmos – deposited film
- Mechnisms
  - Reduced scattering normal to current flow
  - Reduced effective mass due to band curvature changes

1790 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 51, NO. 11, NOVEMBER 2004

A 90-nm Logic Technology Featuring Strained-Silicon

Scott E. Thompson, *Member, IEEE*, Mark Armstrong, Chis Auth, Mohsen Alavi, Mark Buehler, Robert Chau, Steve Cea, Tahir Ghani, Glenn Glass, Thomas Hoffman, Chia-Hong Jan, Chis Kenyon, Jason Klaus, Kelly Kuhn, Zhiyong Ma, Brian Mcintyre, Kaizad Mistry, *Member, IEEE*, Anand Murthy, Borna Obradovic, Ramune Nagisetty, Phi Nguyen, Sam Sivakumar, Reaz Shaheed, Lucian Shifren, Bruce Tufts, Sunit Tyagi, Mark Bohr, *Senior Member, IEEE*, and Youssef El-Mansy, *Fellow, IEEE*

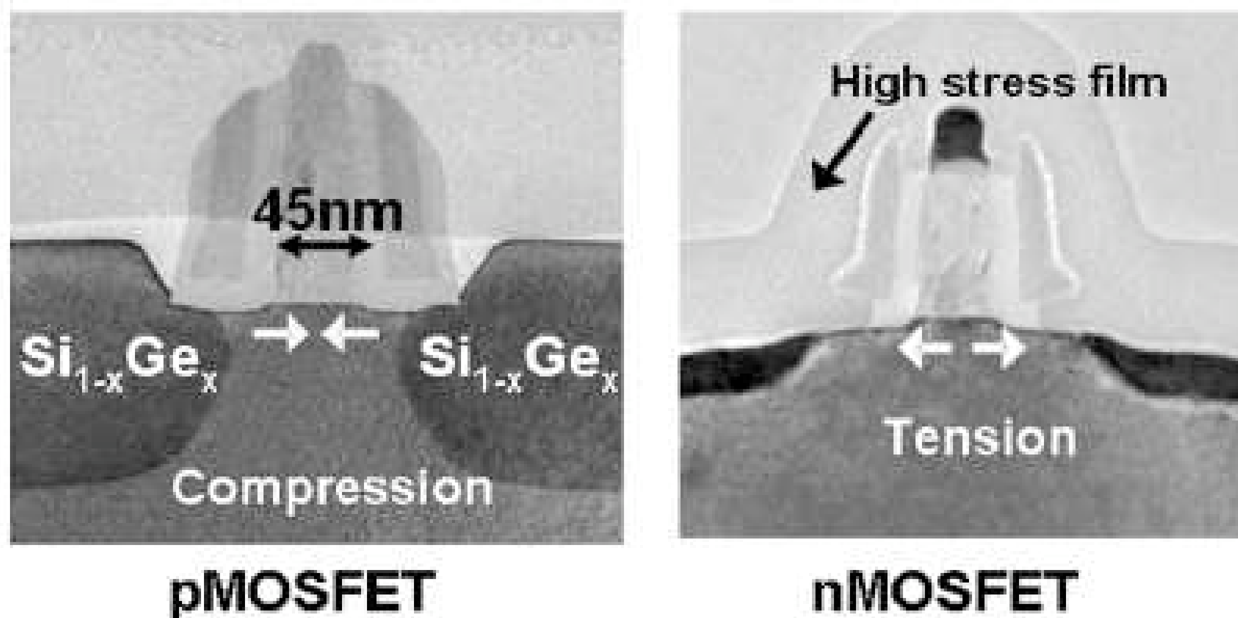
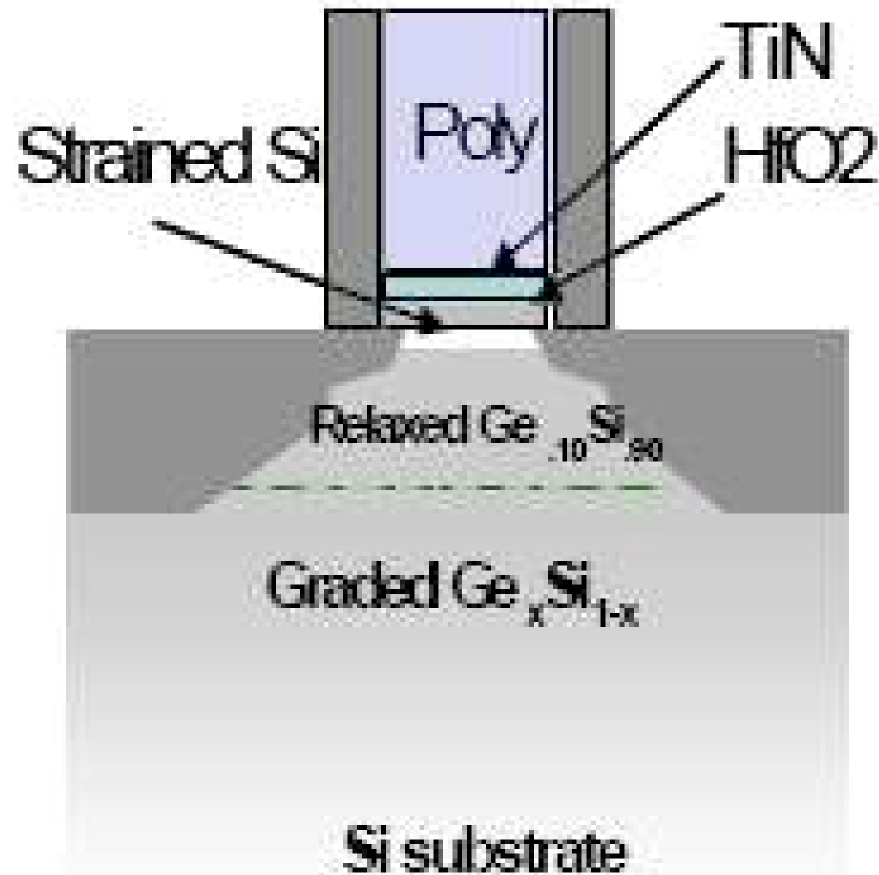


Fig. 2. TEM micrographs of 45-nm p-type and n-channel transistors [4].

High Mobility Si/SiGe Strained Channel MOS Transistors with HfO_2/TiN Gate Stack

S. Datta, G. Dewey, M. Doczy, B.S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar,
M. Metz, N. Zelick and R. Chau

Components Research, Intel Corporation, Hillsboro, OR-97124, USA



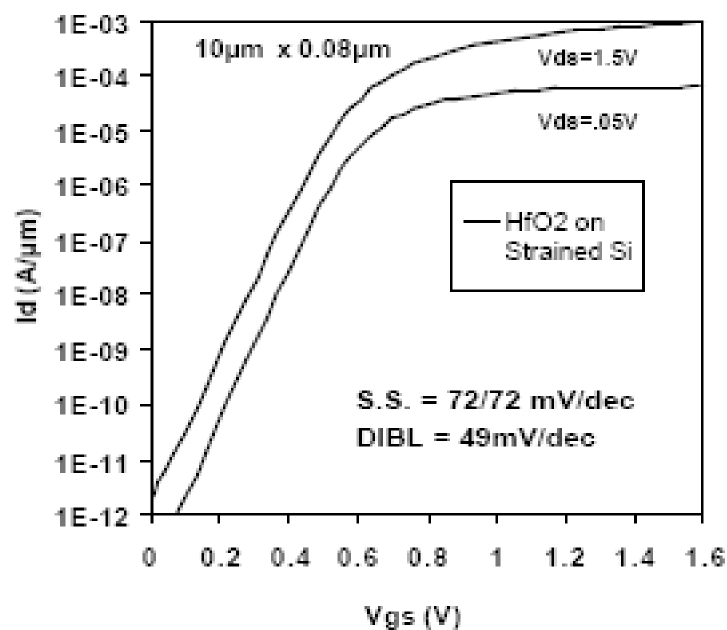


Fig. 11 Id-Vg characteristics of the 80 nm HfO_2/TiN NMOS devices on strained Si showing Ion of 930μA/μm at 1.5V Vds with Ioff of 1pA/um.

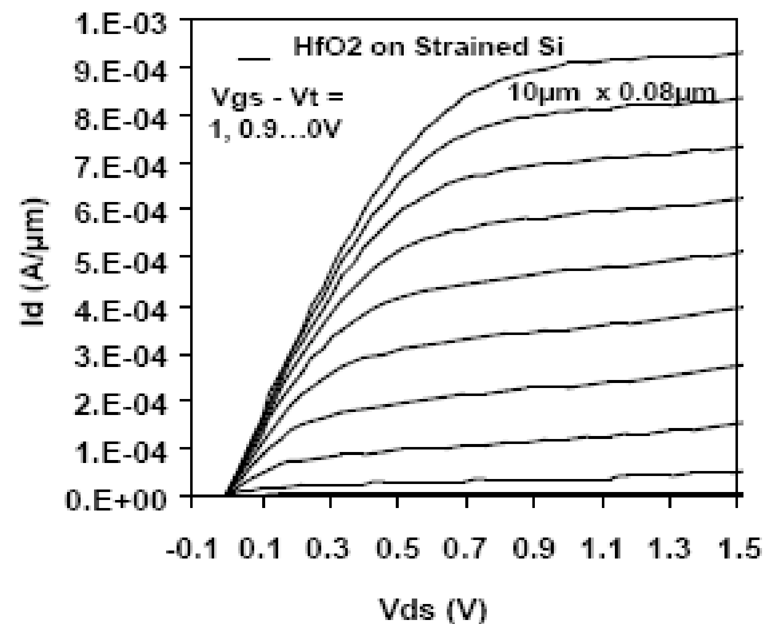


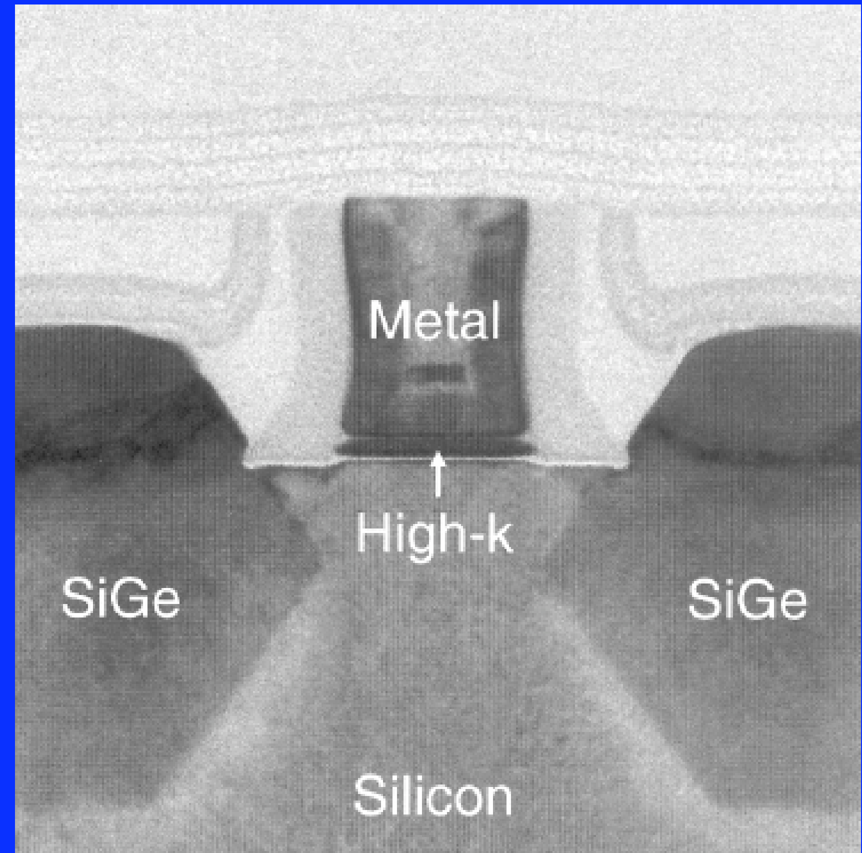
Fig. 12 Id-Vds characteristics of the 80 nm HfO_2/TiN NMOS devices on strained Si (without self-heating correction)

Transistor Features

- 35 nm min. gate length
- 160 nm contacted gate pitch

- 1.0 nm EOT Hi-K
- Dual workfunction metal gate electrodes

- 3RD generation of strained silicon



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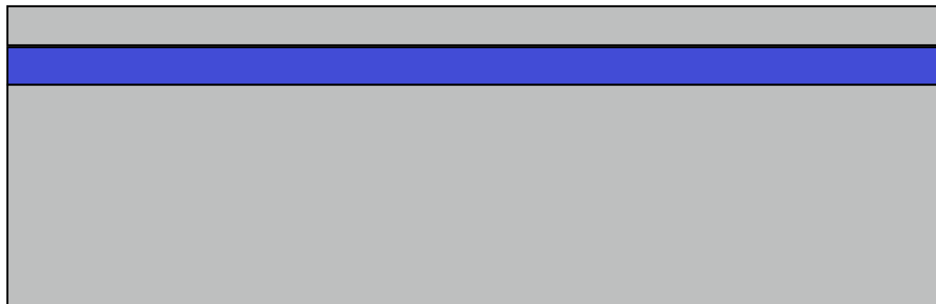
Silicon-On-Insulator (SOI) process

Buried insulator (oxide) layer separates device layer from substrate:

- Reduced parasitic capacitance – high speed
- Improved radiation immunity – space
- Eliminates latch-up
- Source-drain depth set by Si thickness



Si – device layer
Oxide
Si - substrate

SOI Structure

Fully Depleted SOI (FD)

- Si thinner than depletion layer – fully depleted
- Kink effect eliminated
- Short channel behavior improved – get shallow junctions from thin Si layer
- Threshold voltage depends on Si thickness

$$V_T = -V_{offset} + \frac{qN_A t_{Si} d}{\varepsilon_i}$$

- *Si thickness becomes a critical dimension(~10 nm)*

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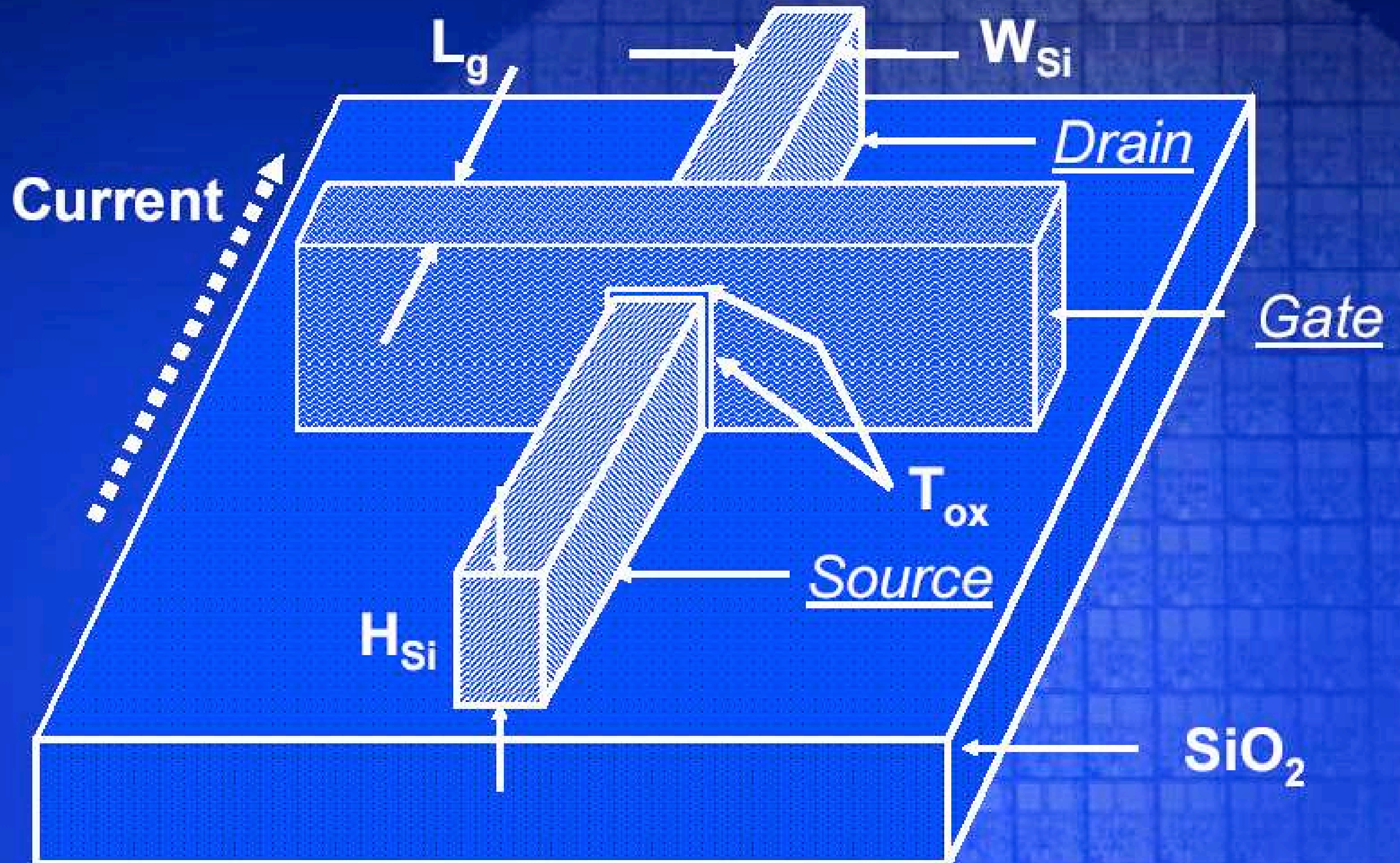
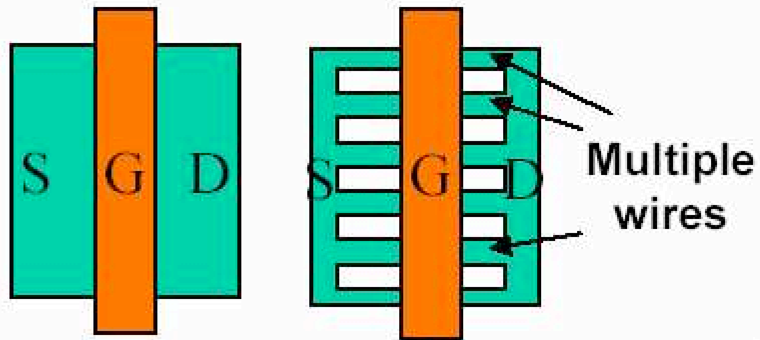
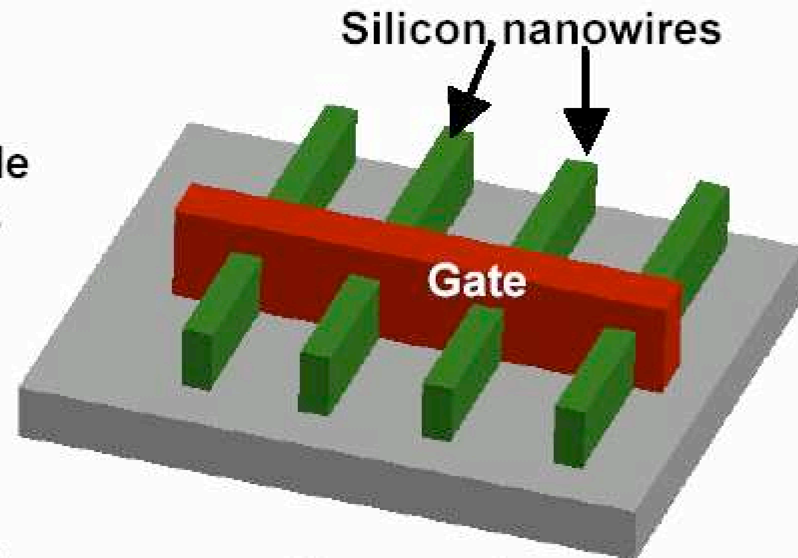
Tri-Gate Transistor Structure

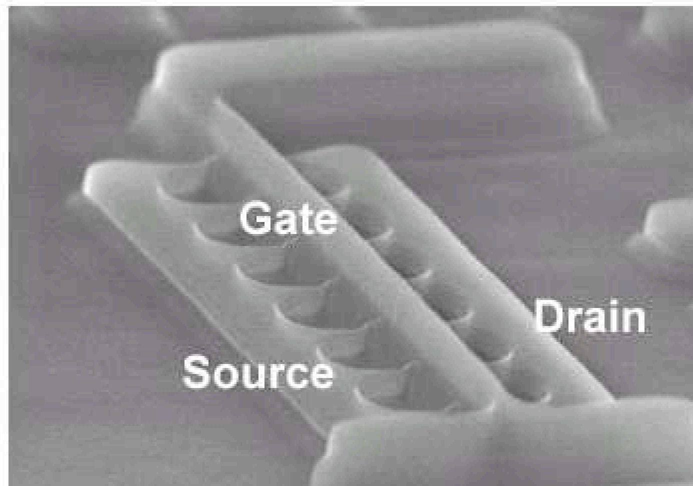


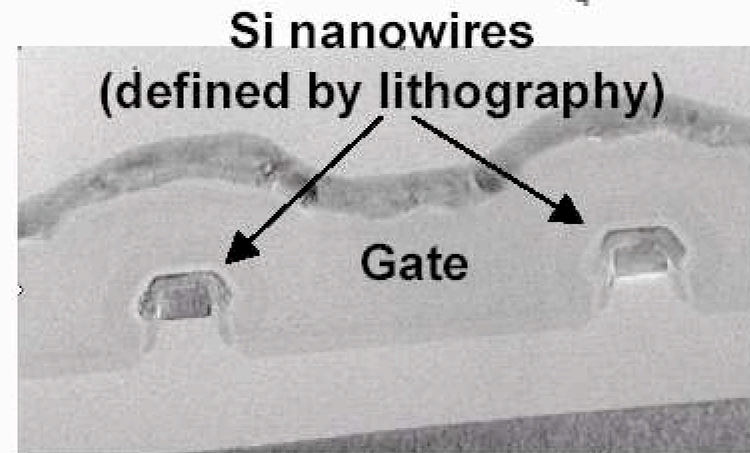
Nano-device Architecture





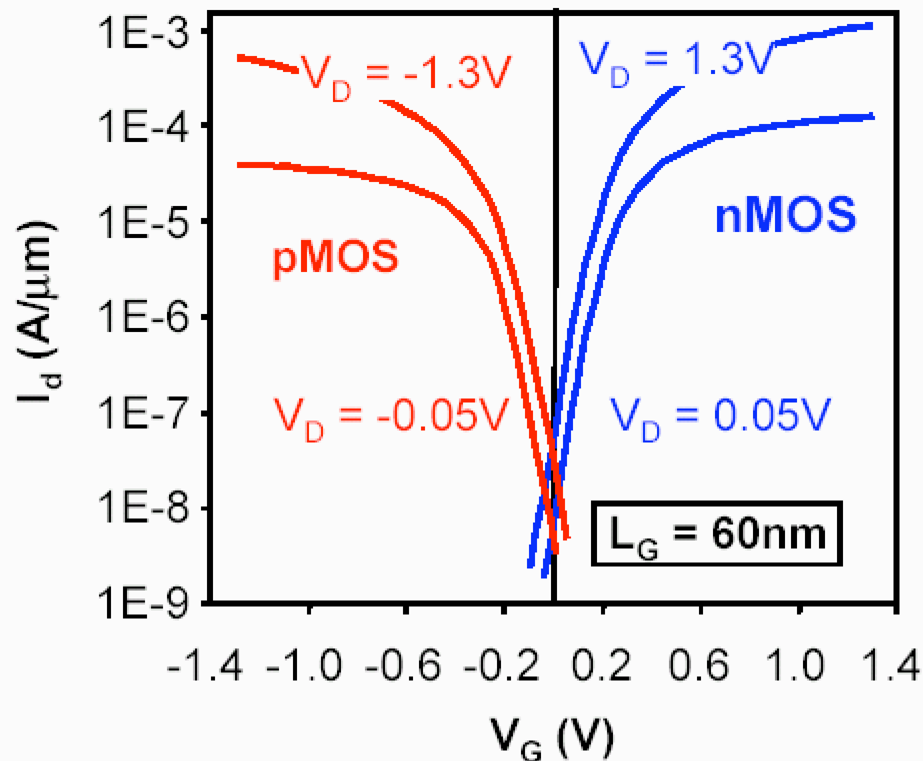
Total Drive Current =
I_d per nanotube/nanowire x no. of tubes/wires



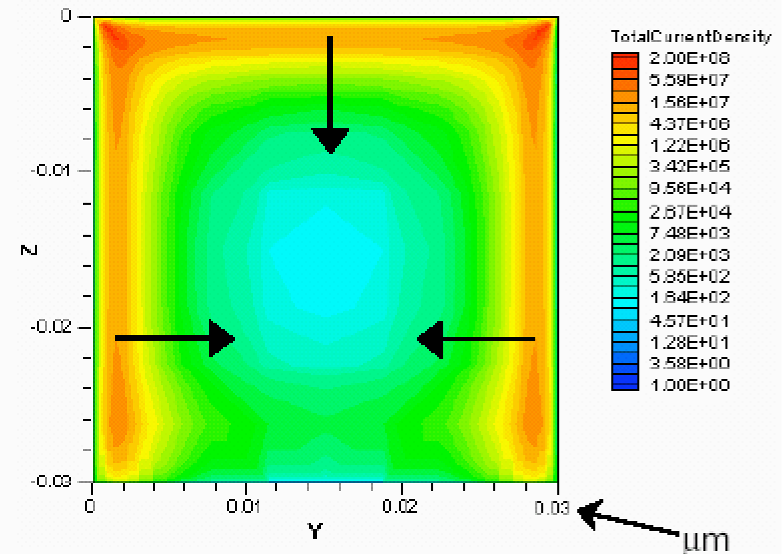


Si nanowire transistor in action:

$L_G = T_{Si} = W_{Si}$ for optimum performance



Simulation of the current density through the device:



Device scaling below ~10nm leaves only "inversion" layer in place

- **Better current density, better control of SCE, better off-state**

ITRS

2007 2010 2013 2016 2019

2005 2006 2008 2009 2011 2012 2014 2015 2017 2018 2020 2021

DRAM 1/2 Pitch: 65nm 45nm 32nm 22nm 16nm

Enhanced mobility (strained Si, etc.)

High-k gate dielectric (all logic types)

Metal gate electrode (all logic types) for planar bulk. Work function near band edges.

Ultra-thin body, Fully Depleted (UTB FD) SOI (HP)

Metal gate electrode for UTB FD SOI and multiple gate MOSFET (Work function near midgap.)

Multiple-gate MOSFET (HP)

Enhanced quasi-ballistic transport

Emerging Research Logic Devices and Circuit/ Architectures (see Emerging Research Devices Chapter)

Research Required | Development Underway | Qualification/Pre-Production | Continuous Improvement

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.