DFE architectures for high-speed backplane applications

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Embedded and look-ahead decision feedback equalisation (DFE) architectures are proposed to overcome the speed bottleneck of DFE design for high-speed backplane applications. DFE design examples simulated in 0.18 μm CMOS technology demonstrate the feasibility of 10Gbit/s operation over a 34-inch FR4 backplane.

Introduction: As data rates increase, transmission suffers from severe eye closure caused by inter-symbol interference (ISI), crosstalk noise, and reflections. Pre-emphasis and analogue equalisation are effective in countering ISI but for some legacy backplanes they amplify high-frequency noise [1]. PAM-4 alternatives [2] alleviate ISI but have interoperability issues and suffer from reduced voltage margins that exacerbate crosstalk effects. DFEs [3, 4] can overcome the drawback of high-frequency noise amplification. In a DFE, prior data decisions are multiplied by tap weights and subtracted from the received signal, eliminating post-cursor ISI. The bottleneck of DFE is that the feedback loop delay should be less than half Baud period. In this Letter, DFE architectures and high-speed design techniques are proposed to overcome the bottleneck.

DFE architectures: Multi-tap half-rate DFE: A half-rate DFE one post-tap is proposed in [3], where the design has only one post-tap. This DFE is extended to be multi-tap, as shown in Fig. 1a, adding retiming DFFs with interleaved clocking. Current-mode logic (CML)-based DFFs are used instead of sense-amplifier-based DFFs to achieve the highest speed. The CML-based equaliser (EQ) is shown in Fig. 1b. Timing analysis has shown that adding more taps does not increase the feedback loop delay and the timing constraint is

\[ T_{eq} \leq 1/2T - T_{cq} \]  

(1)

where \( T_{eq} \) is the EQ delay, \( T_{cq} \) is the DFF clock-to-output delay and \( T \) is the Baud period. Therefore the maximum data rate is

\[ f_{\text{max}} = 1/[2(T_{eq} + T_{cq})] \]  

(2)

The DFE can be implemented as part of the phase detector of a CDR architecture, so the DFE circuit overhead is small.

**Fig. 1** Half-rate three-tap DFE architecture; and EQ implementation

\( a \) Half-rate three-tap DFE architecture \( b \) EQ implementation

Embedded DFE: Fig. 2a shows the proposed embedded three-tap DFE, where the EQ is embedded into a CML latch as shown in Fig. 2b. The first DFF (EQ_Latch + Latch) output of one branch is connected to the EQ_Latch input of the other branch. This feedback forms the first post-tap connection. The second DFF output forms the second post-tap input to the EQ_Latch in the same branch. This embedded architecture removes the EQ delay from (1) and the timing constraint is reduced to

\[ T_{eq} \leq 1/2T \]  

(3)

**Fig. 2** Embedded three-tap DFE architecture; and CML latch with EQ embedded

\( a \) Embedded three-tap DFE architecture \( b \) CML latch with EQ embedded

Look-ahead DFE: To overcome the timing constraint caused by the feedback loop delay, the look-ahead scheme [4] can be used. Parallel calculations are made for the two anticipated decisions: either ‘HIGH’ or ‘LOW’; and then a multiplexer (MUX) is used to select the actual choice. Fig. 3a shows the look-ahead two-tap DFE architecture and Fig. 3b shows the proposed CML-structured MUX. The timing constraint of the look-ahead DFE is

\[ T_{eq} \leq T - T_{MUX} \]  

(4)

where \( T_{MUX} \) is the delay of the data selection MUX.

**Fig. 3** Look-ahead two-tap DFE architecture; and CML MUX

\( a \) Look-ahead two-tap DFE architecture \( b \) CML MUX

Embedded look-ahead DFE: The concept of embedded DFE can be applied to the look-ahead DFE. Fig. 4a shows the proposed embedded look-ahead two-tap DFE, where the MUX is embedded into the CML latch (Fig. 4b). The timing constraint is reduced to a single flip-flop delay, i.e.

\[ T_{eq} \leq T \]  

(5)

Although the maximum data rate can be achieved with this architecture, the hardware overhead may become prohibitive when a large number of taps is required.

**Simulation results:** Without any equalisation, the eye diagram at the far-end of a 34-inch FR4 backplane for PRBS15 data transmitted at 10Gbit/s is completely closed. In the following DFE design examples, pre-emphasis or pre-equalisation are used to reduce the required number of DFE taps. As shown in Fig. 5a, a link is set up with a three-tap FIR pre-emphasis, the backplane, and an embedded three-tap DFE (Fig. 2a). The clock is set to 5 GHz, with rise/fall time set to 30% of...
the clock period. HSPICE simulation results of 0.18 μm CMOS implementation are presented here. Fig. 5b shows the eye diagram at the input to DFE (far-end of channel) and the eye diagram of recovered data at the output of DFE. The equalised even and odd eye diagrams at EQ_Latch output are shown in Fig. 5c. As shown in Fig. 6a, a similar link is set up with a two-stage analogue pre-equaliser, followed by an embedded look-ahead two-tap DFE (Fig. 4a). The pre-equaliser has a highpass gain boost of 12 dB at 5 GHz. Fig. 6b shows the eye diagram at the input to DFE and the eye diagram of recovered data at the output of DFE. The eye diagrams at EQ_Latch output are distorted and thus not shown.

Fig. 4 Embedded look-ahead two-tap DFE architecture, and CML latch with MUX embedded
a Embedded look-ahead two-tap DFE architecture
b Latch with MUX embedded

Fig. 5 Embedded DFE: link setup; eye diagrams at DFE input and output; eye diagrams at EQ_Latch outputs
a Link setup  b Eye diagrams at DFE input and output

Fig. 6 Embedded look-ahead DFE: link setup; eye diagrams at DFE input and output
a Link setup  b Eye diagrams at DFE input and output

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