Conclusion: A top-down design methodology for CPTL circuits has been shown and applied to logic circuit design. The simulation results proved that the method can be applied to digital VLSI circuits efficiently. This design method has the silicon area, delay and low power advantages of PTL. It has also been used for digital signal processing (DSP) chips. It has the simplest way of coding, realisation and simplification with respect to existing methods. The coding can be applied to the 123 DD technique if PTL-based design is required. The simplification process of the 123 DD is more complex to apply than the proposed one. The simplicity and effectiveness advantages of the proposed method make it one of the most efficient CPTL circuit design methods.

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References

Fig. 1 System block diagram of clock synthesiser

Lock detector and window generator: The lock detector of this synthesiser is to prevent the DLL from locking to multiple cycles or zero cycle and to set initial voltage at power on. The operating principle of the lock detector and window generator is shown in Fig. 2, where

\[ S_1 = \sum_{i=0}^{n} P_i + \bar{P}_{i+1} \]
\[ S_2 = \bar{P}_{n+1} \]

It produces two signals, \( V_{\text{under}} \) and \( V_{\text{over}} \) for the total delay time smaller than \( T - (n - 1)/n \) or larger than \( T - n/2 \), where \( T \) is the period of the reference signal. Otherwise, the window generator outputs a negative pulse \( P_{\text{win}} \) at each rising edge of the delayed signal \( P_n \) as shown in Fig. 2, which is used in the phase comparator and charge pump.

Fig. 2 Operating principle of lock detector and window generator

Phase comparator and charge pump: To minimise the in-lock error, the phase comparator and charge pump use a new technique, in which paths from \( P_0 \) and \( P_n \) to \( L_{\text{up}} \) (the output of the charge pump) are short, symmetric and matched. The resolution of this circuit can thus be higher than that of conventional circuits. The operating principle is shown in Fig. 3. The circuit acts on rising edges of \( P_0 \) and \( P_n \). A pulse generator (PG) provides two negative pulses at these rising edges. The phase error can be obtained by comparing the output of two

Reduced in-lock error DLL-based clock synthesiser with novel charge pump phase comparator

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A reduced in-lock error and low jitter delay-locked loop (DLL)-based clock synthesiser employing a novel phase comparator and charge pump is proposed. HSPICE simulation results show the performance of this DLL-based synthesiser to be significantly better than that of other reported circuits. In particular, it has smaller in-lock error and lower output jitter.

Introduction: Delay-locked loops (DLLs) are preferred for many applications because of their unconditional stability and ability to lock rapidly [1]. Since the noise in the voltage-controlled delay line (VCML) does not accumulate over many clock cycles, DLLs usually can offer jitter performance superior to that of phase-locked loops (PLLs) [2]. However, the jitter performance of DLL-based synthesisers depends strongly on the in-lock error, the error between the reference clock and the delayed clock when the loop is in lock. In this Letter we propose a DLL-based clock synthesiser which uses a novel phase comparator and charge pump to greatly minimise this in-lock error. It also includes a lock detector to eliminate the need for initialising the control voltage and it automatically recovers when the DLL loses lock.

System operating principle: The system block diagram of the clock synthesiser is shown in Fig. 1. A VCDL includes multiple identical delay cells, each having two delay stages within and able to generate one pulse the width of which is one half of its delay time upon application of the rising edge of the input signal. When the total delay of these cells \((D_1 + D_2)\) is exactly equal to one period of the reference signal, the signal combiner generates an output signal the frequency of which is an integer multiple of the frequency by combining pulses coming from each of the delay cells. In addition, there are two extra delay cells, one working as an input buffer and another at the end of the delay chain to provide load balance. Except for variance of delay among these delay cells, most output jitter is due to the in-lock error between \( P_0 \) and \( P_n \).
The integrators, IntU and IntD, placed at the output of the pulse generator. The integrators are reset by the rising edge of $V_{out}$ and kept at zero until $V_{out}$ returns to a low voltage in the next cycle. There is no need to make the widths of $P_0$ and $P_0$ wide to solve the dead-zone problem as is necessary in conventional circuits. The width ratio of pulses $P_0$ to $P_0$ is therefore larger, easing the requirements for the phase comparator. A pulse control feedback (PCFB) adjusts the amplitudes and widths of $P_0$ and $P_0$ pulses to ensure two integrators and the voltage comparator work correctly, and it makes the circuit insensitive to process parameter variation, temperature variation, and so on.

![Fig. 3 Operating principle of phase comparator and charge pump](image)

The schematic diagram of the pulse generator is shown in Fig. 4. $P_0$ and $P_0$ are applied to the gates of transistors $M_2$ and $M_3$, respectively, thus $M_2$ or $M_3$ can be turned on when $P_0$ or $P_0$ goes high. Transistors $M_2$, $M_3$, and $M_2$ form two current mirrors to ensure that currents through $M_2$ and $M_3$ are same as the bias current through $M_2$. The $M_2$ bias current is controlled by $V_{diss}$ and $P_0$- $P_0$. $V_{diss}$, coming from the pulse control feedback circuit, adjusts the widths and amplitudes of $P_0$ and $P_0$ pulses. This is achieved by tuning the bias current flowing through $M_2$. Following a falling edge of $V_{out}$, $M_2$ provides a bias voltage for $M_2$ and $M_3$. Next, the circuit waits for the rising edge of $P_0$ or $P_0$, which pulls down $P_0$ or $P_0$ separately. Once both $P_0$ and $P_0$ are high, $P_0$ and $P_0$ return to a high state simultaneously.

A schematic diagram of integrators, feedback, and voltage comparator circuits is shown in Fig. 5. The two pulses $P_0$ and $P_0$ are integrated to obtain signals $V_0$ and $V_0$. The voltage comparator obtains the error signal between the two pulses, or between $P_0$ and $P_0$. A pulse control feedback circuit dynamically adjusts the voltage of $V_{out}$ (the control signal of the pulse generator as shown in Fig. 4). With this feedback circuit, the high level amplitudes of $V_0$ and $V_0$ are slightly higher than the threshold voltage of NMOS when the loop is in lock.

![Fig. 4 Schematic diagram of pulse generator](image)

Simulation results: To demonstrate the performance of the synthesizer described above, a 9-time $(n = 9)$ clock synthesizer was designed in a CMOS 0.18 μm technology and simulated using HSPICE. Its input frequency is 200 MHz and the output frequency is 1.8 GHz. In lock, in-lock errors between $P_0$ and $P_0$ were obtained as shown in Fig. 6a, and the calculated output jitter is shown in Fig. 6b. The RMS value of the in-lock error is 0.1 ps and that of the output jitter is 0.7 ps, indicating far better performance than that of other reported circuits [1].

**References**


**High quality 80 Gbit/s InP DHBT selector and its use for NRZ-RZ conversion**

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A high speed selector IC fabricated in self-aligned InP DHBT technology is presented. Circuit measurements at 80 Gbit/s (measurement setup limitations) show very good eye opening (0.56 ps RMS time jitter, low rise and fall times). Circuit operation at 40 Gbit/s NRZ to RZ converter was also characterised.