On \( \Delta \Sigma \) Fractional-N Frequency Synthesizers

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Abstract—\( \Delta \Sigma \) fractional-N frequency synthesis achieves low phase noise performance while relaxing the Phase-Locked Loop (PLL) design constraints and reduces the desired channel spacing. This paper reviews the recent advanced techniques on the implementation of fractional-N frequency synthesizers and discusses their advantages and disadvantages. It also addresses the design options and the associated trade-offs.

I. INTRODUCTION

Design of PLL-based frequency synthesizers using an integrated VCO faces a loop-bandwidth optimization issue. A large loop bandwidth is desirable to provide agile frequency switching and VCO phase-noise reduction. At the same time the loop bandwidth must be significantly smaller than the reference frequency to attenuate the associated frequency spur and to maintain the loop stability. In the integer-N architecture the use of a higher reference frequency facilitates a small channel spacing. The fractional-N architecture relaxes the above trade-off and provides the ability to use a higher reference frequency (and thus greater loop bandwidth) while having the desired channel spacing.

II. \( \Delta \Sigma \)FRACTIONAL-N FREQUENCY SYNTHESISERS

A. Advantages and Drawbacks

In fractional-N frequency synthesizers the output frequency can be a fractional ratio of the reference frequency. The frequency resolution is finer than the reference frequency. Given the same channel spacing, a fractional-N synthesizer can be designed with a higher loop bandwidth than an integer-N design. Higher loop bandwidth results in faster frequency switching and thereby allowing dynamic bandwidth techniques to be used more efficiently [1,2]. In a dynamic bandwidth approach, the loop bandwidth is set to be wider than desired when the PLL is outside of the lock-in-range to obtain a faster settling time during the transient mode. A higher reference frequency results in a higher comparison frequency that in turn relaxes the PLL requirements in terms of the noise contribution and the reference spur.

For a given channel spacing and a targeted output phase noise, the PLL noise requirement is smaller in the fractional-N architecture with respect to an integer-N counterpart due to the smaller divider modulus. The reference spur is also less dependent on the leakage current and the non-ideal effects of the charge-pump [3].

There are several approaches to designing fractional-N synthesizers that are all more complex as compared to the integer-N counterparts. Fractional-N can be inherently more spurious and may exhibit worse phase noise performance due to quantization issues. The wider loop bandwidth imposes more stringent requirements on the in-band phase noise but also increases the reference frequency, phase detector (PD) noise and the discrete spurious level.

B. Applications

Using a fractional-N architecture permits the realization of both phase and frequency modulations directly in the synthesizer. This eliminates the need for up-conversion mixers in the transmitter and allows for a reduction of the power consumption [4,5]. There is an emerging application in new radio systems like TETRA, in which channel spacing and switching time specifications cannot be met with ordinary integer-N synthesizers. The high resolution of the fractional-N architecture can be used for automatic frequency control (AFC), Doppler correction or other features that require tuning. This architecture is also used to relax the trade-offs in conventional integer-N synthesizers using the same bandwidth.

C. Synthesizer Architecture

The challenge of designing a fractional-N frequency synthesizer involves trade-offs amongst phase noise, frequency switching speed, loop bandwidth, frequency resolution, tuning bandwidth and power consumption. The fractional frequency multiplication factor is achieved by manipulating the divider modulus (which is inherently an integer) in a way that the average division ratios make the desired fractional ratio. Fig. 1 shows a typical \( \Delta \Sigma \) fractional-N frequency synthesizer. The output sequence of an over-sampling \( \Delta \Sigma \) modulator (i in Fig. 1) is used to control the divider modulus. The high pass transfer function of a \( \Delta \Sigma \) modulator pushes the close-in phase noise to high frequencies where the low-pass loop filter can remove part of this high frequency noise that is outside of its bandwidth [7]. This method can generate an arbitrarily fine frequency with digital modulation and when compared to other methods, it is less sensitive to analog mismatch and process, voltage and temperature (PVT) variations, has less spurious output and relatively better phase noise. It does however, have a relatively high complexity and power consumption.

![Figure 1. \( \Delta \Sigma \) fractional-N synthesizer](image-url)
modulators increases at higher rates. Each integrator introduces a zero
the quantization error and removing the spurious frequency
components from the synthesizer output spectrum.

Nonlinearties like PD & ad-zone and charge-pump
noise, steady state, and
these architectures are possible but the digital implementation is more
common in fractional-N synthesizers.

The source of in-band noise can be the jitter in digital logic,
noise folding due to a non-linearity, charge-pump current
noise, offset current noise and reference noise. Digital logic
jitter is the major contributor to in-band noise [10] and includes
the contributions from the divider, the PD and reference path.
Nonlinearities like PD dead-zone and charge-pump
nonlinearity modulate high frequency quantization noise into
the signal bandwidth. This phenomenon is called noise folding and can be suppressed by controlling the distribution of the
quantization noise and limiting the PD operation region to its
linear section [10].

III. ΔΣ MODULATORS

In fractional-N synthesizers, the input of the ΔΣ modulator is
usually a digital word representing the desired fractional value
while the output is a stream of single-bit or multi-bit numbers
used to control the divider modulus. This stream has an
average equal to the desired fractional ratio. Therefore in
steady state, the VCO output frequency would be forced to the
desired fractional multiplication of the reference frequency. All
ΔΣ modulators involve quantization noise but such noise is
larger in single bit modulators. Multi-bit ΔΣ modulators may
be used to reduce the quantization noise. The order of the ΔΣ
modulator is equal to the number of integrators in the structure.
Each integrator introduces a zero at the origin in the transfer
function, and thus shapes the noise spectrum in the frequency
domain. Converting the frequency to phase removes the zero
from first order ΔΣ modulator preventing it from randomizing
the quantization error and removing the spurious frequency
components from the synthesizer output spectrum [7].

By selecting higher order ΔΣ modulators, the spurious
energy is spread out and shaped to resemble high frequency
noise, which is removed by the low-pass nature of the loop
filter. The low frequency components of the quantization non-
linearity error are filtered more by a higher order ΔΣ
modulator. The output noise spectral density of higher order
modulators increases at greater rates per unit frequency,
resulting in greater signal to noise ratio (SNR) in the base-band
bandwidth at the cost of higher out-of-band noise. When higher
order modulators are used, the PLL requires extra poles in the
loop filter to suppress the quantization noise at the high
frequency. From experience both in-band and out-of-band
noise affects the synthesizer performance but the high
frequency noise is difficult to suppress with a finite number of
PLL poles [8]. Second and third order ΔΣ modulators are
typically used for fractional-N synthesizers [4][5][7][8][16].

IV. ΔΣ MODULATORS ARCHITECTURES

The choice of an appropriate ΔΣ modulator structure for
fractional-N synthesis requires the consideration of many
factors including noise shaping, spurious content of the output
spectrum, output levels, loop filter order and circuit
complexity. Both analog and digital implementations of these
architectures are possible but the digital implementation is more
common in fractional-N synthesizers.

In a digital implementation, an accumulator acts as an
integrator and a comparator. As it also has a feedback path, it
can be considered as a compact first order ΔΣ modulator [16].
Digital ΔΣ modulators do not have non-linearities. They are
stable as long as the word lengths are large enough to avoid
overloading. Cascade digital modulators do not suffer from
mismatch and noise leakage from the front stage (unlike the
analog counterparts) and multi-bit quantizers usually do not
suffer from non-linearity.

High order modulators can be realized with interpolative and
MASH (Multi-stage noise shaping) architectures. The MASH
architecture uses a cascade of lower-order structures to
construct a high-order modulator [17]. It is typically
constructed using a cascade of first order modulators or a
combination of first and second order modulators. The MASH
modulator produces a multi-bit output, which must control a
multi-modulus divider. In general a multi-bit modulator can
achieve more desirable noise shaping for frequency synthesis.
A programmable counter can serve as a multi-modulus divider
but such a counter is hard to implement for very high speeds.
An estimate for the hardware complexity of a MASH
modulator can be found in [18].

MASH offers a simpler high order architecture with no
stability problem and tends to generate widespread high
frequency bit patterns that imposes more stringent
requirements on PD design. Intensive switching activity of the
MASH ΔΣ modulator increases the high frequency noise and
causes larger instantaneous phase error. A fourth-order MASH
provides a higher order of noise shaping (~80 dB/dec) but it has
almost twice the complexity of a third-order MASH and
consumes greater power. As shown in Fig 2 and Fig. 3, the

Figure 2. A digital MASH 1-1-1-1 ΔΣ modulator
third-order MASH can be realized as a MASH 1-1-1 or a MASH 1-2, which are a cascade of three first order modulators or a cascade of one first-order and one second-order (Ritchie [19]) modulator, respectively. MASH 1-1-1 and MASH 1-2 exhibit the same order of noise shaping however the MASH 1-2 can be designed to have four output levels instead of eight as in the MASH 1-1-1 [18]. The big disadvantage of MASH 1-2 is that it only allows the input to operate over about 75% of the whole fractional range [18].

A single-loop (also called interpolating or single-stage) ΔΣ modulator introduces smaller phase noise and can provide either a single-bit or a multi-bit output. It is subject to instability and a smaller input range. The latter can be eliminated with a multi-bit quantizer in a digital implementation. A typical third-order single-loop multiple-feedback ΔΣ modulator is shown in Fig. 4. The quantizer output is limited to three levels and the feedforward branches can be truncated to reduce complexity.

Another version of a single-loop uses multiple-feedback [20] is shown in Fig. 5. In order to obtain a reasonable stable input range a large number of quantization levels is required (i.e. nine in this example). The bit length of the adders preceding the accumulators are much shorter than the accumulators themselves [21]. A tone free output can be achieved at the cost of high output levels. However, the output levels are more concentrated than in the MASH 1-1-1 [22].

The wide-spread output pattern of a MASH modulator makes the synthesizer more sensitive to the substrate noise coupling since the turn-on time of the charge-pump in the locked condition increases. This can be reduced by limiting the output range of the modulator [8]. The smaller on-time of the CP in a single-loop modulator makes it less sensitive to noise coupling from the substrate and power supply. Due to intermodulation in the PD and the CP, the noise at freq/2 folds back to a lower frequency similar to the multi-bit ΔΣ ADCs. For a single-loop modulator, noise at freq/2 is much lower and thus its noise leakage due to non-linearities is also lower. Although the ideal case in-band phase noise is lower for the MASH ΔΣ modulator due to the higher phase error introduced, only a small non-linearity is sufficient to increase the in-band noise more than expected from a single loop modulator. The single-bit high-order modulator has a dead-band problem due to the limited input range of the quantizer in synthesizer applications. The non-ideal effects at the band edges can be reduced by extending the input range with a multi-level quantizer [8].

V. IMPLEMENTATION ISSUES

The division modulus is modulated by the ΔΣ output, at the desired mean value as well as by the shaped high frequency quantization noise. The main advantage of the fractional-N synthesizer is the independence of the choice of the reference frequency and the PLL bandwidth. To ensure that the modulator does not corrupt the rms phase error, the dynamic range of the modulator must be higher than that of the frequency synthesizer [8]. The dynamic range of a frequency synthesizer is defined as the ratio of the largest possible frequency change to the smallest. The largest frequency change is the full frequency range of the modulator within the modulus range. In fractional-N synthesis applications, the ΔΣ input is a constant number but the output sequence may not be long enough to be of practical use. The periodic nature of a short output sequence creates spurious tones in the synthesizer output. A simple way to achieve a longer output sequence is to increase the bit-length of the input, but this increases modulator complexity and the power consumption. To reduce the fractional spurs resulting from the limited output sequence, some perturbation is imposed in the ΔΣ output sequence by applying a dithering signal from a pseudo-random generator to the input. In [18] the carry-in input of the adder is used in a feedback path to randomize the input. In [25], a 14 dB suppression of spurious tones is achieved by using the 3 output bits of the MASH modulator as a dithering signal to replace the least significant bits of the modulator.

VI. SIMULATION ISSUES

The long simulation time for fractional-N frequency synthesizers is mainly due to two causes. One is the high output frequency of the synthesizer that forces the simulator to use a high simulation sample frequency. Second, fractional-N
synthesizer has a non-periodic behavior in steady state, which prevents the use of methods developed for periodic steady-state conditions [11].

In [12] the area conservation principle is used to convert a continuous time phase-frequency detector (PFD) output to a discrete time sequence and to use a uniform step size for simulation. Considering the fact that the overall dynamics of the loop changes typically at much lower frequency than the VCO output, assuming the VCO and the divider to be one block allows the use of a much smaller sampling period in the simulation [12].

VII. MULTI-PHASE FRACTIONAL-N SYNTHESIZERS

Although a multi-modulus divider can achieve any arbitrary fractional ratio, the minimum phase jump at the divider output is still equivalent to one VCO period. In [13,14] a finer resolution is achieved by interpolating the phases using analog techniques such as multi-phase VCOs having a phase jump smaller than one VCO period at the divider output. The phase mismatch (i.e. the phase inaccuracy of the multi-phase VCO outputs) gives rise to fixed spurs when the output phases are selected sequentially. In [15] modulation is used in combination with phase interpolation to eliminate the spurs. A smaller phase jump at the divider output decreases the equivalent quantization step size and consequently the equivalent quantization noise of the modulator. Thus this approach exhibits lower phase noise than a multi-modulus approach. A block diagram of a multi-phase fractional-N synthesizer is shown in Fig. 6.

VIII. CONCLUSION

This paper provides an overview of \( \Delta \Sigma \) fractional-N frequency synthesis. A discussion is provided on the structures of \( \Delta \Sigma \) implementations outlining the merits of techniques, implementation and simulation issues.

REFERENCES


