A Gigahertz Cyclic Injection DLL Clock Generator with an Infinite Acquisition Range

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Abstract—This paper presents the implementation of a cyclic injection DLL based clock generator with an infinite acquisition range and low timing jitter, low phase noise performance. A novel switching scheme with a resettable divider is designed to synchronize the operation of the other blocks in the circuit and to eliminate the need of a start-up or locking detection circuitry. The phase noise performance is improved by injecting the reference edge periodically. Programmable multiplication ratios from 13 to 20 are achieved with an output frequency range of 900 MHz to 2.9 GHz. The circuit is implemented in TSMC 0.18μm CMOS technology. The measured cycle-to-cycle timing jitter at 2.5GHz is 2.49 ps (rms) and 20 ps (pk-pk), and the phase noise is -119dBc/Hz at 1MHz offset for a carrier frequency of 2.756 GHz.

I. INTRODUCTION

An excellent timing jitter performance is crucial for the clock generation unit of high-speed data communication systems. Traditionally the phase-locked loops (PLLs) dominate in the field of timing generations in the SOC application. In recent years, however, the delay-locked loops (DLLs) based clock generation is under exploration because it exhibits a better noise performance compared with the PLL counterpart. Except the non-jitter accumulation in the voltage-controlled delay line (VCDL), DLLs are normally easier to design since it is normally a first order system, which is unconditionally stable. The loop filter can be a small valued capacitor, so the DLL is easy to be integrated in a small area. To date, many DLL based clock generators are reported and their implementations mainly fall into two typical categories. One is based on a multiple-stage VCDL (to generate multi-phase signal) and an edge combining circuit (to combine those multi-phase signals) [1] [2], and the other type is based on cyclic reference edge injection in a VCO-like VCDL [3] [4]. Compared with the first type, clock generator, the second type of clock generators can achieve programmable frequency multiplication ratio more easily with a frequency divider and eliminate the mismatch among multiple delay stages. Since the phase error does not accumulate in DLLs, without specific measures, both structures may suffer from false locking because the phase/frequency detector may compare wrong edges. In contrast, PLL has no such concern since the phase error of the VCO can accumulate over cycles, and by slipping some cycles, the loop can always acquire lock as long as the initial state is in the acquisition range of the PLL.

This paper proposed a new DLL clock generator with a control logic employing a new switching scheme working together with a frequency divider and the PD in the clock generator with cyclic edge injection. With the new control logic scheme, the PD can always compare the correct edges and produce correct tuning signal so that the correct lock of the DLL can be guaranteed for any initial VCDL delay value without a start-up or auxiliary complex locking detection circuitry.

II. CIRCUIT OPERATION

The block diagram of the proposed clock generator is shown in Figure 1. It comprises of a PD, a charge pump (CP), a Mux, a programmable divide-by-N divider, a switching logic, a VCO-like VCDL and a loop filter. The combination of the VCDL, the Mux and the frequency divider is equivalent to the multi-stage VCDL without the stage mismatch. When the control signal of the Mux is 0, the reference signal is connected to the VCDL so that the reference edge can be fed into the delay line. When the control signal of the Mux is 1, the VCDL is configured as a VCO and the reference edge circulates in this ring oscillator until the control signal goes back to 0 and the next clean reference edge is injected into the VCDL to cancel out the phase error accumulated in the previous cycles. This injection act happens every period of the reference or every N cycles of the VCO output, where N is determined by the division ratio of the divider. One output of the VCO vref is applied to the PD to compare the phase with the reference edge, and UP and DN signals are generated to tune the VCO frequency toward the correct value. To minimize the output jitter caused by the switching activities of the loop, the signal foff is used as the final output of the clock generator because
The correct comparisons (as arrows shown in Figure 2) are guaranteed with proper design of the PD and the switching logic circuit, which also determines when the reference edge is injected and when the frequency divider is reset. Consequently, the n-th or more generally, the n-th rising edge of the output is always locked to the reference edge that was just injected, and the use of any type of frequency detection circuitry or start-up circuitry is eliminated.

III. CMOS IMPLEMENTATION

A. The divide-by-N divider

The frequency divider divides its input \( f_{ref} \) by a given number, and it can be reset when necessary. After a given number of cycles are counted, the switch logic circuit will generate a reset signal at the time when the new reference edges synchronize the frequency divider with the reference by forcing it to count from zero. Without the reset, the frequency divider keeps dividing its input signal, so each output cycle corresponds to a certain number of its input cycles. By implementing a count-to-2 circuit, the switch logic circuit determines when a given number of VCDL cycles are completed.

The frequency divider consists of three divide-by-2/3 dividers and control qualifiers. By programming the three inputs \( P_0, P_1 \) and \( P_2 \), multiple division ratios can be achieved. The ratio can be calculated as

\[
N = \sum_{i=0}^{2} 2^i \cdot P_i + 8 \quad (1)
\]

Multiple integer division ratios from 8 to 15 can be obtained from the equation. Due to the delay from the output of the VCO, the divider and the switching logic, to the MUX switch, the actual multiplication ratios of the frequency synthesizer are from 13 to 20.

B. The VCDL and MUX

The VCDL, which is also configured as a VCO, is based on 3-stage current starved inverters. It provides two outputs, \( f_{ch} \), the output of the last delay stage, and \( f_{chb} \), the output of the second delay stage. Because every reference period, the switching activity changes the load of the last VCDL stage, which drives more loads, the signal \( f_{ch} \) is chosen to be used as the clock generator output. The input of the VCDL is either \( f_{ref} \) or \( f_{ch} \) depending on the switching signal \( MUX_{re} \). If \( MUX_{re} \) is high, \( f_{ch} \) is passed through the VCDL, and the output is propagated as \( f_{chb} \) in the VCDL. If \( MUX_{re} \) is low, the reference rising edge is injected into the VCDL. In lock condition, this reference edge injection happens once within every reference period.

The MUX is a selecting switch of the VCDL. It consists of two pass gates and \( f_{ch} \) or \( f_{chb} \) is passed through the gates controlled by signal \( MUX_{re} \) which is generated in the switching logic.
C. The Switching logic

The switching logic works as a timing control unit by synchronizing the operation of the PD, the Mux, and the divider. The schematic is shown in Figure 3. It consists of six DFFs with reset function and two delay elements. There are four inputs $d_{out}$, $s_{out}$, $s_{in}$, and $r$. The reference $f_{ref}$ is used to synchronize the loop with the reference by providing switching signals $PD_{sw}$, reset, and $Max_{sw}$. The signal reset not only resets the divider, but the other two DFFs (the count-to-2 circuit) in the switching logic as well.

For the purpose of self-correcting of the loop for arbitrary initial VCDL delay values, a new switching scheme is employed in the synchronized operation timing for the PD, the Mux and the divider by generating corresponding switching signals. Figure 4 shows the timing sequence when the loop is in lock.

On the rising edge of the reference signal, the reset signal (the output of DFF1) goes high and keeps high for a certain time depending on the delay of the delay element $d_{in}$. Then the divider is reset and its output $d_{out}$ goes down. On the rising edge of $f_{ref}$ (a rising reference edge was just injected), the reset goes down, and the divider starts to count from zero again upon the falling edge of reset every reference cycle.

The timing of signal $PD_{sw}$ is critical as it helps self-locking for the case where the VCDL delay is too large shown in Figure 2 (c). From section A, the $d_{out}$ has two rising edges at every reference cycle, which can be observed in Figure 4. DFF1 and DFF2 form a count-to-2 circuit. At the first rising edge, the output of DFF1 is high, and at the second rising edge when the counting-to-N is reached, the DFF2 goes high. Once the rising edge of $f_{ref}$ arrives, the reference signal is injected, and $PD_{sw}$ goes high and keeps high for a certain time determined by the delay value of $d_{out}$ and the reset signal that is enabled once a reference edge is injected. Consequently, signal $PD_{sw}$ is enabled right before the rising edge of the n-th rising edge and disabled right after the injected reference rising edge. This characteristic ensures that the PD always compares the n-th output rising edge with the correct reference rising edge.

Due to the circuit delay, the divider is not reset immediately after the counting-to-N is finished, and the starting-to-count is not effective after the falling edge of the reset either. So five more output cycles recirculate in the VCO, resulting in a multiplication ratio larger than the calculated division ratios of the frequency divider.

The $Max_{sw}$ is triggered to be high in DFF6 at the rising edge of $f_{ref}$ when the $PD_{sw}$ is high. In other words, the Mux input is connected to the reference after the n-th falling edge of $f_{ref}$ and connected to $f_{ref}$ after the rising reference edge.

D. The charge-pump phase detector

The schematic of the phase detector is shown in Figure 5. It is based on a dual-DFF based PFD with a switching function controlled by signal $PD_{sw}$ from the switching logic. To properly operate with the proposed switching scheme, the control signal $PD_{sw}$ does not simply disable/enable the PFD. The operation of the PFD (for the case $N=6$) is illustrated in Figure 5. It produces two outputs, UP and DN, with the width difference corresponding to the phase difference of its inputs. The signal UP is enabled by the rising edge of $f_{ref}$ no matter whether the $PD_{sw}$ is enabled or not. However, the DN signal is enabled at the rising edge of $f_{ref}$ only if the $PD_{sw}$ is...
enabled. Both of them are reset at the same time after a certain delay when both \( UP \) and \( DN \) are enabled. In addition, to guarantee a correct initial state of the PFD, the reset also happens at each falling edge of the \( PD_{in} \) which turns low right after a new reference edge is injected and shows up as the falling edge of \( f_{id} \) as shown in the figure.

As illustrated in Figure 6, it is obvious that the correct phase difference can always be obtained no matter how much the initial delay of the VCDL is. Consequently, an infinite delay acquisition range of the DLL is achieved.

IV. MEASUREMENT RESULTS

The circuit is implemented in CMOS 0.18\( \mu \)m technology and tested with a synthesized reference signal from an RF signal generator. Figure 7 presents the measured jitter histogram. The measured cycle-to-cycle RMS edge jitter is 2.49 pS and the peak-to-peak value is 20 pS at the 2.5 GHz output with the multiplication ratio of \( N = 19 \). The measured phase noise at the output of 2.756 GHz is -119.8 dBc/Hz at 1 MHz offset, and approximately -110 dBc/Hz at 100 kHz offset as shown in Figure 8. Similar results are achieved for other frequencies tested. Supplied by a 1.8 V DC source, the circuit consumes approximately 19 mW for an output frequency of 2.5 GHz, and the output frequency range is from 900 MHz to 2.9 GHz. The active area including the capacitors is 0.07 mm\(^2\). Figure 9 shows the main part of the chip microphoto.

V. CONCLUSION

A cyclic injection DLL based clock generator with an infinite acquisition range is presented. The proposed switching scheme working with the frequency divider eliminates the operation of other blocks to eliminate the need for a start-up circuitry or a frequency lock detection circuitry. With the cyclic edge injection, the phase noise accumulated within N cycles of the output clock is cancelled, and the measured phase noise and timing jitter performance confirms the function and the efficiency of the circuit.

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