Challenges in the design of next generation WLAN terminals

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Abstract— In recent years advancements in the field of wireless communications have generated interest in the deployment of multiple antenna systems (MIMO) for mobile terminals. Next generation wireless local area networks (WLANs) standards such as IEEE 802.11n are based on MIMO and will be operating at bit rates above 200 Mbps. The physical layer (PHY) of the 802.11n supports multiple modulation schemes, multiple antennas configuration, variable code rate and multiple space-time coding schemes. Receiver architecture should be able to support all these features preferably in a single reconfigurable architecture. Besides all these requirements need to be designed and implemented under the strict low power and low complexity (low area) design criteria.

Keywords- MIMO, IEEE 802.11n, reconfigurable hardware

I. INTRODUCTION

The major challenge facing the future wireless communication networks is to provide high data rate wireless access to multiple mobile users at high quality of service (QoS) without increasing the used frequency spectrum. The link reliability in a wireless channel is affected by the fading caused by destructive addition of multipath components and interference from other users.

Multiple-input multiple output (MIMO) wireless technology seems to meet these demands by offering increased spectral efficiency through spatial multiplexing and improved link reliability due to antenna diversity. These improvements come at a significant increase in signal processing and hardware complexity of both receiver and transmitter blocks compared to existing single antenna systems.

Current industry trends suggest that large-scale deployment of MIMO wireless systems will initially be seen in WLANs and in wireless metropolitan area networks (WMANs). Related standards currently under definition include the IEEE 802.11n WLAN standard and the IEEE 802.16 WMAN standard [1]. Both standards define air interferences that are based on the combination of MIMO with orthogonal frequency division multiplexing (OFDM) modulation (MIMO-OFDM). In mobile access, there has been an effort under the International Telecommunications Union (ITU) working group to integrate MIMO techniques into the high-speed downlink packet access (HSDPA) channel, which is a part of the Universal Mobile Telecommunications System (UMTS) standard, as a result MIMO is part of UMTS in Rel. 6 together with HSDPA. Ongoing fourth-generation mobile cellular system pre-standardization efforts also show strong support for a MIMO-OFDM air interface.

Theoretical aspects of MIMO communication have been the focus of many research projects for the past few years and even though there are still a number of open research problems in theory of MIMO wireless, the technology has reached a stage where it can be considered for hardware implementation. Research in practical implementation of MIMO communication is in its early stages and there are many open issues that need to be addressed [5].

In this paper, first we review the 802.11n proposal and summarize hardware design challenges and requirements for future receivers as briefly described earlier in this introduction. We will introduce base band architecture that supports these requirements and we will discuss related implementation challenges associated with these architecture. These design challenges are essential receiver design requirements for next generation wireless terminal.

II. REVIEW OF IEEE802.11N PROPOSAL

A. 802.11n background

In January 2004 IEEE announced that it had formed a new 802.11 Task Group (TGn) to develop a new amendment to the 802.11 standard for wireless local-area networks. The real data throughput is estimated to reach a theoretical 540 Mbits/s, and should be up to 50 times faster than 802.11b, and well over 10 times faster than 802.11a or 802.11g.

Previous competitors TGn Sync, WWiSE, and a third group, MITMOT, merged their respective proposals and formed the Enhanced Wireless Consortium (EWC) [6]. On January 19, 2006, the IEEE 802.11n Task Group approved the joint proposal specification, based on EWC’s specification [7] as the confirmed 802.11n proposal. According to the IEEE 802.11 Working Group Project Timelines, the 802.11n standard is not due for final approval until July 2007.

IEEE 802.11n builds upon previous 802.11 standards (802.11a, 802.11b and 802.11g) by adding MIMO (multiple-input multiple-output) technology. MIMO uses multiple
transmitter and receiver antennas to allow for increased data throughput through spatial multiplexing and increased range and BER performance by exploiting the spatial diversity and space-time block coding schemes like Alamouti coding [2][3]. The proposed block diagram of transmitter is shown in Figure 1.

![Transmitter block diagram](image)

Figure 1. Transmitter block diagram

B. IEEE 802.11n proposal requirements

The Modulation and Coding Scheme (MCS) is a parameter that determines the modulation, coding and number of transmit antennas. MCS is part of the transmitted packet and is used to configure the receiver mode. In the following we will briefly review different receiver operating modes defined in this standard.

1) Spatial Mapping

Spatial mapping block in Figure 1. maps spatial streams to different transmit chains. This may include one of the following mapping options:

- Direct mapping- each sequence of constellation points sent to a different transmit chain.
- Spatial expansion- each vector of constellation points from all the sequences is multiplied by a matrix to produce the input to the transmit chain.
- Space Time Block coding- constellation points from one spatial stream are spread into two spatial streams using a space time block code.
- Beam Forming- similar to spatial expansion, each vector of constellation points from all the sequences is multiplied by a matrix of steering vectors to produce the input to the transmit chains.

Receiver and transmitter should be able to support these mapping schemes.

2) Number of transmitter antennas (spatial streams)

Number of transmitter antennas is variable and can be up to 4 antennas. The receiver should be able to adapt itself to the number of transmitter antennas defined by MCS. This has a major impact on the design of MIMO detector block.

3) Modulation types

Transceiver should be able to support different types of modulation. The modulation types that are supported are BPSK, QPSK, 16-QAM and 64-QAM. It is also possible that different transmitting antennas use different modulating schemes. TABLE I. shows valid combinations of modulation schemes for the 3-antenna mode as defined in the proposal. As it can be seen in this table there are cases that the modulation type of each of the transmitter antennas are different. MIMO detector in the receiver side should be able to decode such asymmetrical cases.

4) Variable code rate

The code rate is a programmable parameter and depends on modulation type and can be set to 1/2, 2/3, 3/4 and 5/6.

5) FEC Decoding

The suggested decoder for forward error correction in this standard is LDPC. LDPC is soft-input decoder and this requires the MIMO detector to be a soft-output detector and preferably an iterative decoder to improve BER performance of the system.

III. IMPLEMENTATION CHALLENGES OF MIMO RECEIVERS

In this section we review the implementation challenges associated with designing MIMO receivers and specifically detector block in the receiver. We divide these challenges into 4 categories.

A. Silicon Area

The performance gains achievable in MIMO-OFDM systems come at a significant increase in hardware complexity, as an example the ASIC described in [8] contains the baseband digital signal processing functional blocks of the PHY layer of a MIMO receiver, including an MMSE ordered-successive interference-cancellation (OSIC) MIMO detector. The die area breakdown of the ASIC according to functional blocks along with die area figures for a corresponding single antenna (SISO) system is summarized in TABLE II. Compared to a single antenna transceiver, the 4×4 MIMO transceiver requires the four-fold replication of most of the functional blocks and in addition a channel-matrix preprocessor for MIMO detection and the MIMO detector itself [5]. The overall chip area in a MIMO receiver increases by a factor of 6. As it can be seen in this table, the total area associated with the MIMO detector is close to 26% of the total area of the MIMO receiver thus optimizing the area of detector will have a significant effect on the overall receiver area.

<table>
<thead>
<tr>
<th>Index</th>
<th>Modulation</th>
<th>Code Rate (Mbps)</th>
<th>Data Rate (Mbits/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>39</td>
<td>16-QAM</td>
<td>QPSK</td>
<td>1/2</td>
</tr>
<tr>
<td>40</td>
<td>16-QAM</td>
<td>QPSK</td>
<td>2/3</td>
</tr>
<tr>
<td>41</td>
<td>64-QAM</td>
<td>QPSK</td>
<td>3/4</td>
</tr>
<tr>
<td>42</td>
<td>64-QAM</td>
<td>16-QAM</td>
<td>1/2</td>
</tr>
<tr>
<td>43</td>
<td>64-QAM</td>
<td>16-QAM</td>
<td>1/2</td>
</tr>
<tr>
<td>44</td>
<td>64-QAM</td>
<td>16-QAM</td>
<td>1/2</td>
</tr>
<tr>
<td>45</td>
<td>64-QAM</td>
<td>16-QAM</td>
<td>1/2</td>
</tr>
<tr>
<td>46</td>
<td>64-QAM</td>
<td>QPSK</td>
<td>1/2</td>
</tr>
<tr>
<td>48</td>
<td>64-QAM</td>
<td>QPSK</td>
<td>1/2</td>
</tr>
<tr>
<td>49</td>
<td>64-QAM</td>
<td>16-QAM</td>
<td>1/2</td>
</tr>
<tr>
<td>50</td>
<td>64-QAM</td>
<td>16-QAM</td>
<td>1/2</td>
</tr>
<tr>
<td>51</td>
<td>64-QAM</td>
<td>QPSK</td>
<td>1/2</td>
</tr>
<tr>
<td>52</td>
<td>64-QAM</td>
<td>16-QAM</td>
<td>1/2</td>
</tr>
</tbody>
</table>
B. Performance (throughput)

The main goal in MIMO communication is to increase the overall data throughput of the communication system. One of the limiting factors in achieving this goal is the processing speed of the MIMO detectors. There are three main implementation platforms for implementing detection algorithms. Burg in [3] and [4] analyzed the computational performance of each of these platforms as well as the processing requirements of some of the previously implemented MIMO algorithms. Figure 2. ([3], [4]) shows the result of their analysis. The regions of operation of three main implementation platforms are shown in the graph, on the horizontal axis of the chart the number of data items to be processed per second is depicted and the vertical axis provides the number of operations per data item. The diagonal lines represent constant numbers of operations per second. As it can be seen, dedicated hardware implementations are more than 10 times energy efficient than general purpose microprocessors and 10 times more efficient than programmable DSPs. The MOPs/mw ratio for MIMO receivers are well fitted within the dedicated hardware performance range.

C. Power consumption

There is a strong demand for high level MIPS in 2010 and beyond driven by the high demand signal processing applications. Power will be the limiting factor to reach this goal. By comparing the power consumption in Intel processors in recent years we can see an increase of more than 2% in power for every 1% increase in performance, which results in a poor MIPs/Watt ratio [14]. The same argument is valid for DSPs processors. The MOPs/mw ratio for different signal processing applications is shown in Figure 3. As it can be seen, dedicated hardware implementations are more than 100 times energy efficient than general purpose microprocessors and 10 times more efficient than programmable DSPs. The MOPs/mw ratio for MIMO receivers are well fitted within the dedicated hardware performance range.

D. Flexibility

Next generation receivers should be able to support multiple operating modes set by transmitter during transmission of each packet. A review of IEEE 802.11n proposal in the previous section shows that receiver should be able to support programmable number of transmitter/receiver antennas, modulation schemes, spatial mapping and coding rate. As mentioned in sections B and C programmable processors and DSPs are not viable choices for implementation of MIMO receiver due to their low performance and relative high power consumptions. On the other hand dedicated hardware architectures are not programmable devices. Reconfigurable hardware architectures like FPGAs, overcome the performance limitations of DSPs while still maintaining to some extent the flexibility of a programmable device. However, cost and power dissipation of FPGAs are more than ASIC based implementations. Dedicated ASICs on the other hand provide much lower power consumption and used silicon area but they lack the programmability and flexibility that exists in programmable devices and FPGAs.

One solution to overcome these problems is to have multiple hardware architectures to support different operating modes and switch between these architectures as operating mode changes. The major drawback with this approach is increased silicon area and power consumption which are limiting factors in portable devices. The other option is to apply the reconfigurable hardware design methodology in designing MIMO receivers.

The concept of reconfigurable computing has been around since the 1960s, when Gerald Estrin’s [9] landmark paper proposed the concept of a computer consisting of a standard processor and an array of “reconfigurable” hardware. The main

<table>
<thead>
<tr>
<th>Component</th>
<th>Area (mm²)</th>
<th>4x4 MIMO</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDC, DUC</td>
<td>0.5</td>
<td>1.9</td>
</tr>
<tr>
<td>AGC</td>
<td>0.1</td>
<td>0.6</td>
</tr>
<tr>
<td>FDE, FOC, FSU</td>
<td>0.3</td>
<td>1.3</td>
</tr>
<tr>
<td>Modulator, IFFT</td>
<td>0.9</td>
<td>1.4</td>
</tr>
<tr>
<td>Frame buffers</td>
<td>-</td>
<td>2.3</td>
</tr>
<tr>
<td>Channeld estimation</td>
<td>0.1</td>
<td>1.29</td>
</tr>
<tr>
<td>QR decomposition</td>
<td>-</td>
<td>1.23</td>
</tr>
<tr>
<td>QR memory</td>
<td>-</td>
<td>0.9</td>
</tr>
</tbody>
</table>

Table 2. Area of Baseband Functional Blocks [8]
processor would control the behavior of the reconfigurable hardware. The reconfigurable hardware would then be tailored to perform a specific task. Once the task was done, the hardware could be adjusted to do other tasks. This resulted in a hybrid computer structure combining the flexibility of software with the speed of hardware [10].

IV. RECEIVER ARCHITECTURE

The architecture of the receiver is shown in Figure 4. Due to the power and throughput limitations discussed in the previous section, the baseband processing block consists of a combination of dedicated HW blocks and programmable processors. PHY processor can be implemented using embedded processors. PHY processor analyzes the physical layer parameters and reconfigures the dedicated HW blocks. The MIMO decoder in this architecture is an iterative MIMO detector/decoder and as a result the MIMO detector should be a soft-output MIMO detector. There has been a number of architecture in the literature related to soft MIMO detectors [11][12][13], but the issue of configurability has not been addressed yet. The major architectural issue in designing MIMO detector is how to address the following requirements preferably in a single architecture:

- MIMO detection when transmitted symbols from different antenna are modulated using different modulation schemes.
- Variable number of transmitter and receiver antennas.

These issues are more interesting when the detector is tree search based detector. The other major issue in designing detector is how to support multiple spatial mapping in detector.

V. CONCLUSION

Future generation wireless standards support multiple operating modes and configurations. Programmable processors and DSPs are the best choices for implementation of baseband processing blocks since they are easily programmable. The major issues with programmable platforms are their processing speed and power consumption. We concluded that the optimal architecture for receiver would be a combination of embedded processor and reconfigurable dedicated hardware blocks.

REFERENCES