Modeling, Simulation and Analysis of High-Speed Serial Link Transceiver over Band-Limited Channel

Bo Wang¹, Dianyong Chen¹, Bangli Liang¹, Jinguang Jiang² and Tad Kwasniewski¹
¹DOE, Carleton University, 1125 Colonel By Dr., Ottawa, ON, K1S 5B6, Canada
²ISS, Wuhan University, Wuhan, Hubei, China 430079
E-mail: {bwang, ddchen, bliang, tak}@doe.carleton.ca, jgjiang95@yahoo.com.cn

Abstract

This paper presents an integrated modeling, simulation and analysis technique for high-speed serial link transceiver over band-limited channel. The Verilog-A behavioral modeling blocks, transistor-level circuits based on the BSIM models, and the backplane channel with .s4p format model were simulated simultaneously in Cadence Spectre environment. The output data were post-processed with Matlab for performance analysis. Compared with HDL-based modeling scheme and event-driven modeling method, the proposed modeling method provides the effective system level verification in the integrated environment, even with real transistor-level circuits included.

1. Introduction

High-speed serial link transceiver systems often employ complicate communication theories, such as transmission lines, equalization theory, and clock and data recovery etc. [1] The backplane is a complex environment which includes at least 11 different components, each of which has its own impedance variations [3]. For the data rate at 5-Gb/s or above, the signal integrity of the serial data communication is a significant problem in the serial link transceiver design. Signal integrity issues, such as skin effect, dielectric loss, reflection, inter-symbol interference (ISI), and crosstalk etc., are to be analyzed in the system level design. To overcome these channel impairments, system design must be developed on accurate and efficient models. The accurate modeling of such a complex system is necessary for system verification. On the modeling of the system, the signal-integrity related problems can be understood and minimized. An HDL-based modeling method is proposed in [1], and an event-driven method is published in [2]. This work proposed a Verilog-A modeling technique, and the transceiver is analyzed in Cadence Spectre environment with acceptable simulation time and accuracy.

The next section describes the band-limited backplane channel environment, and its characteristics and model. Section 3 presents the modeling method for the serial link transceiver in Cadence Spectre environment. Section 4 provides the simulation and analysis results of a modeled serial link transceiver system. The conclusion is drawn in Section 5.

2. Backplane environment

2.1. Backplane model

As data rates through the backplane approach several giga-bits/s or above, the signal integrity issues become more significant. The band-limited backplane channel can not be treated as a channel with lumped capacitances, and it must be a lossy transmission line. The main signal integrity issues with the band-limited backplane channel are:

- Skin effect and dielectric loss (frequency dependent)
- Reflection (due to impedance discontinuities)
- Crosstalk (near-end and far-end)
- Jitter and skew (due to the time dispersion), etc.

The accuracy of the model for the complex channel is very important for system-level simulation and analysis. There are several methods for modeling the backplane or the other band-limited channels, such as with RLCG per unit length, four-port S-parameter, and transfer function with zeros and poles in Verilog-A etc. The four-port S-parameter model (touchstone format) is the most extensively used method, and a typical backplane .s4p format model file is shown in Figure 1. The data in the model file are based on the measurement results of the backplane from an S-parameter vector network analyzer (VNA). The characteristics of the insertion loss, return loss and
crosstalk etc. can be obtained accurately from this model file.

2.2. Backplane channel characteristics

With the four-port model file, the backplane channel can be simulated and analyzed with an n4port cell, which can load the model file, in Cadence environment. Normally, the frequency range in the model is from 50-MHz to 15-GHz with 50-MHz step. The response below 50-MHz and above 15-GHz can be linearly interpolated to cover full-range response over larger bandwidth. The S-parameter analysis of the backplane channel is shown in Figure 2. The insertion loss (S21), the return loss (S22) and the crosstalks (S23, S24) are compared in the plot. Fortunately, the main distortion of the high-speed serial link transmission over backplane channel, which would be a lossy transmission line, is from frequency-dependent magnitude loss.

3. Wireline transceiver modeling

Recently, there are many papers about the serial-link transceiver system analysis and modeling published from academic and industrial researches [1]-[7]. In paper [1] from Rambus, the system was modeled with Matlab script, Perl script and verilog code. The s4p channel model is converted to over-sampled verilog FIR model. The analysis is based on verilog. In addition, Matlab RF toolbox provides a method to synthesize the s4p model file to a Verilog-A file with zeros and poles in the transfer function. After channel model conversion on the above two methods, the impedance matching properties for the channel can not be represented accurately. In this paper, we proposed a Verilog-A modeling method in Cadence Spectre environment using s4p channel model without conversion, and the output data can be post-processed with Matlab.

3.1. Verilog-A modeling method

The Verilog-A modeling methodology is shown in Figure 3. The backplane channel is modeled with the s4p format model, and the transmitter (Tx) and receiver (Rx) can be modeled with Verilog-A or transistor-level circuits (BSIM model based). The input signals are single pulse or PRBS data, the PRBS data is a piece-wise linear (PWL) text file generated from Matlab. The entire modeling system can be simulated in Spectre. The transient, S-parameter or AC, etc. analyses are...
3.2. Wireline transceiver system

Based on the above modeling methodology, a typical 10-Gb/s backplane wireline transceiver is constructed. The system schematic is shown in Figure 4. In this system, the backplane channel is modeled with a four-port transmission line, which is based on the s4p model file, with 50-Ω termination resistance for impedance matching. The transmitter can generate PRBS random data or single pulse at 10-Gb/s rate. A 5-tap DFE equalizer, which is modeled with Verilog-A, is in the receiver (Rx), and a low-pass filter with transistor-level transmission gate (BSIM model) and parasitic capacitance to simulate the on-chip parasitic poles. Therefore, the transceiver integrated channel model, Verilog-A model and BSIM model in the common environment without the need of the data conversion.

There are two Verilog-A delay cells on the top, which are used to delay the input and received signals with the intention for comparison. The two Verilog-A blocks on the bottom are used to sample the received signal on the data center and edge, and saved to a data file for performance analysis.

The equalizer in the receiver is a traditional 5-tap decision-feedback equalizer (DFE), as shown in Figure 5. It is a fixed coefficients 5-tap DFE, which is modeled with Verilog-A, and the block is constructed according to the real circuit structure. The feedback input gain stage is used to simulate the automatic gain control (AGC) stage in the real circuit for adjusting the signal level. Each delay cell is a one symbol rate delay (100-ps for 10-Gb/s) for the symbol-spaced FIR filter. Due to the post-cursor ISIs cancellation property of the DFE, the fixed tap coefficients can be directly obtained from the impulse response without difficulty. The Verilog-A modeled slicer is a comparator to recover the digital level from the equalized signal. The slicer output is connected to the feedback input on the top-level schematic and closes the feedback loop.

4. Simulation results

4.1. Impulse response in wireline transceiver

With the above wireline transceiver modeling, it can be simulated in Spectre for system analysis. The 100-ps impulse response of the wireline transceiver system is analyzed first, as shown in Figure 6. The insertion loss (S21) of the channel is shown in the figure, it has about -20 dB loss in magnitude at 5-GHz (Nyquist frequency at 10-Gb/s). In the transient analysis, the 100-ps input pulse is attenuated in magnitude and dispersed in time at the receiver side, which is severely distorted. The post-cursor ISIs are reduced at the sampling time after the DFE equalizer.

The spectrum analysis and comparison of the impulse response is shown in Figure 7. For equal comparison, the signal spectra are normalized to the DC magnitude. The 100-ps input single pulse spectrum has null at 10-GHz (the 10-Gb/s baud rate) and -3.87dB in magnitude at 5-GHz. The magnitude of the received pulse spectrum at 5-GHz is about -25.4dB, and the high loss of the received signal is generated from the band-limited channel. The DFE equalizer is used to compensate the channel loss and reduce the post-cursor ISIs. The spectrum of the equalizer pulse has -11 dB loss in magnitude, which is equivalent to compensating about -14.4 dB loss at 5-GHz.
4.2. Transient analysis with PRBS input

The transient analysis with PRBS random data input is shown in Figure 8. The input signal is PRBS-11 serial data at 10-Gb/s. The input signal is delayed by 5.4-ns for comparison with the received signal at the same time point. For the input pattern “010101”, it corresponds to the highest frequency component of the signal and the magnitude loss is the largest. The received signals are severely attenuated and distorted, and the most difficult to detect the symbols from the entire received signal stream. On the DFE equalized signals, they are compensated in time domain and the logic values are separated for making the decision with enough signal-to-noise ratio. The slicer output is the recovered data. Compared with the input, the receiver can recover the signals without errors.

The eye diagrams of the received and equalized signals are shown in Figure 9. Due to the inter-symbol interference (ISI) from the frequency dependent loss of

![Diagram](image-url)
the channel, the eye of the received signals is totally closed, and the clock and data cannot be recovered from the severely distorted signals. After the DFE equalizer, the eye of the equalized signals is opened and the vertical eye opening at the data center is around 224-mV, which is large enough for the decision circuit to recover the digital data at an acceptable BER.

Figure 9. The eye diagrams of the received signal and equalized signal.

5. Conclusion

An integrated Verilog-A-based modeling and analysis technique with Matlab for post-processing is applied to a serial wireline transceiver over high loss backplane at 10-Gb/s data rate. The proposed technique achieves an efficient modeling and analysis for the complex transceiver in the system level. With the help of Matlab, the signals are easily analyzed in time and frequency domain. The significant advantage of the modeling method over the others is that the transistor-level blocks can be simulation with the behavioral modeling blocks in the same environment. The transistor-level circuits can be verified separately in the transceiver system. The proposed modeling technique is more accurate than HDL-based and event-driven methods, especially for high-speed circuits.

6. References


