Abstract—A high modulation efficiency laser diode/modulator driver (LDD/MD) is designed for low-cost optical access networks using shunt peaking active inductors and direct-coupled topology to boost the bandwidth, to improve modulation efficiency, and to reduce the silicon area. It provides a maximum modulation current of 74mA or a maximum modulation voltage of 3.9V through an equivalent 50Ω load. Fully-open optical eye diagrams were observed at bit rate up to 1.25-Gb/s when it used as a LDD or a MD. The maximum RMS jitter is 38ps. The 0.4mm² chip consumes only 470mW in 5V 0.6µm standard CMOS.

Index Terms—Monolithic, High Modulation Efficiency, CMOS, Laser Diode / Modulator driver.

I. INTRODUCTION

With the rapid development of optical access networks, high performance, low cost optical transmitters (TXs) are needed. Therefore, it is possibly the best choice to realize such optical TXs in CMOS. CMOS technologies are playing an increasingly important role in high performance ICs used in optical fibre communications due to their low production costs, high yields, and high integration density [1]-[4]. In the past years, other laser diode drivers with higher costs were realized using resistive-load or transistor active-load, which usually consume more power [1], more chip area [1]-[3]. In general, large voltage drop over LDD makes it difficult to reduce the power supply voltage of the LDD driver below 3.3V. Furthermore, for reliability and application reasons, high power supply CMOS drivers providing large modulation current for laser diode driver (LDD) or high modulation voltage for modulator (MD) are indispensably needed.

In this paper, a LDD/MD using on-chip shunt peaking active inductors and direct-coupled topology is implemented in 0.6µm CMOS for low-cost 1.25-Gb/s optical transmitters.

II. CIRCUIT DESIGN

The schematic diagram of the proposed LDD/MD is shown in Fig.1. The direct-coupled, fully differential circuit consists of an input level-shifter, two amplifying stages and an output stage. The whole circuit is fully balanced using differential amplifiers to maximize its operating speed and to minimize undesired noises.

Fig.1. Schematic of the proposed LDD/MD circuit.

The upper nMOS transistor pair in each amplifying stage is a differential current amplifier. The lower transistor forms the current source for the nMOS transistor pair. The active inductors pair made up of nMOS pair and resistor pair is used as loads. Active inductors with low Q value are used here to boost the bandwidth due to the following reasons: Firstly, high Q value, high inductance on-chip spiral inductors are not easily obtained; Secondly, on-chip spiral inductors inevitably consumed very large chip area; Thirdly, high Q value is not indispensable for wide band amplifiers and the Q value is determined by the poly-silicon load resistors that are connected in series to the inductors; Lastly, active inductors are very compact, easily fabricated and have very good immunity to process, voltage and temperature variations. A differential source follower pair to realize the functions of level-shifting and impedance transforming is omitted here to reduce power dissipation and chip dimension. Thus, direct coupled topology is employed in this design. The input level shifter implemented through a group of 5K high resistance (HR) poly-silicon resistors and a pair of 50Ω low resistance (LR) poly-silicon resistors provides...
the function of DC level shifting and input impedance matching. In this work, identical 5k HR resistors in the level-shifter are employed to obtain an accurate input common-mode level and a more accurate DC bias voltage for current sources. Because DC level offset can be eliminated using identical HR resistors with an equal resistance tolerance resulting from inevitable process variation rather than dissimilar HR resistors with different resistance tolerances. In addition, parasitic inductors of bonding wires for output stage can be properly used to reduce the jitter, rise time of output signal pulse and to enlarge the bandwidth of this DD/MD.

Due to very large output current/voltage swing of the LDD/MD, most of the devices have large aspect ratios (W/L). This will necessarily result in increased parasitic capacitance, especially in critical nodes, which strongly impacts the high speed operation of the LDD/MD. Multiple-finger structure offering nearly 50% reduced source and drain area is employed for all large transistors to minimize parasitic capacitance. Special attention has been given to keep routes as short as possible while using large width to meet the requirement of current density and to minimize parasitic inductance. Great care also has been taken as to virtually avoid large area overlap between supply and signal lines. For the purpose of effective biasing and minimization of substrate bouncing, substrate contact arrays have been extensively used. In addition, double metals which composed ground lines, supply lines and other DC bias lines are used in large area as MIM (Metal-Isolator-Metal) capacitors to cancel undesired noises. Therefore, the performance of this circuit is improved greatly due to all design techniques mentioned above.

III. CIRCUIT FABRICATION

The proposed LD/MD in 0.6µm double-poly double Metal N-well CMOS technology was designed and fabricated in CSMC Semiconductor Co., Ltd. The microphotograph of the die is shown in Fig.2. The chip dimensions including bonding pads (0.1mm×0.1mm) are 0.6mm×0.65mm. On the chip, only one tenth of the total chip area in the middle region is used for the active part.

Fig.2. Microphotograph of the fabricated LDD/MD.

IV. MEASUREMENT RESULTS

The performance of the fabricated LDD/MD is evaluated via on-wafer probing on uncut wafers employing CASCADE MICROTECH probe station, an ADVANCEST D3186 Pulse Pattern Generator, an ADVANCEST R6142 Programmable DC Voltage/Current Generator, a ROHDE&Schwarz SMP04 Signal Generator (10MHz-40GHz), an Agilent 83430A Lightwave Transmitter, an Agilent Lightwave Multimeter and an Agilent Infiniium DCA 86100A Wide-bandwidth Oscilloscope. A low threshold 1.55µm wavelength InAsP/InGaAsP strained multi-quantum well laser diode and a Mach-Zehnder LiNbO3 external modulator are used to observe output optical signals.

The block diagrams of evaluation setup of the realized LDD/MD are illustrated in Fig. 3. The LDD driver provides modulation current and bias current for the used laser diode. The MD driver is used to drive a MZ modulator which has a single-end RF input. If a differential MZ modulator is used, the measured result of this differential MD driver should be much better.

The DC current of the LDD/MD under a single supply of 5V is less than 94mA, corresponding to a power dissipation of 470mW. The circuit has been tested using an input PECL of 500mV_pp at different bit rates. The measured eye-diagrams at the bit rates of 625-Mb/s and 1.25-Gb/s from one single-ended output of the LDD/MD are shown in Fig. 4. The modulation current range at each single-end output of LDD is 0-74mA corresponding to an optical modulation amplitude of 1.24mW. The maximum modulation voltage for MD is over 3.95V_pp corresponding to a 425µW optical modulation amplitude with a 2.15V internal DC bias for the output stage. This driver circuit with a wide input common-mode level range from 1.4V to 3.8V can operate well with different modulation current/voltage outputs under a single supply voltage ranging from 4.5V to 5.5V. Moreover, the temperature coefficient of this driver is only 0.06mA/°C for LDD or 5mV/°C for MD with an operating temperature ranging from -40°C to +85°C.
In Table I, optical measurement data shows the performance of the implemented LDD/MD. The RMS jitter of output optical signal from the driven laser diode and the modulated Mach-Zehnder LiNbO$_3$ external modulator is no more than 38ps, the extinction ratio is larger than 5.5dB, and the SNR ranges from 18.5dB to 27.5dB. From tested eye-diagrams, we can come to a conclusion that the performance of the fabricated chip verges on the anticipant result and can operate at a bit rate up to 1.25-Gb/s.

V. CONCLUSION

A LDD/MD is realized in CSMC 0.6µm CMOS for optical access networks. It uses two stages amplifier with on-chip shunt peaking active inductors to boost the bandwidth without consuming large chip area. The 3.95V$_{pp}$ modulation voltage for laser diode and 74mA modulation current supplied by this LDD/MD result in fully-open optical eye diagrams at the bit rate of 1.25-Gb/s. It can be used as either LDD or MD in OC-24/STM-8 optical transmitters consuming only 470mW.

REFERENCES


Bangli Liang (M’06) received his M.S Degree in Materials Science from Suzhou University in 2000. In 2000 he joined Shanghai Automobile Electronics Engineering Center, where he was engaged in the development of super high speed compound semiconductor devices and ICs. In 2001, as a Director Assistant and Project Engineer, he joined Institute of Radio Frequency and Optoelectronics ICs Southeast University, Nanjing, China. Since 2000, he has developed 24 high-speed chips for data communication systems in CMOS and published 20 journal papers and 18 conference papers in CMOS ICs design, semiconductor device process and won the best post paper award of the 7th International Conference on Solid-State and Integrated-Circuit Technology, 2004. Now he is a Ph.D candidate in VLSI at Carleton University, Ottawa, Canada.