Transmitter Equalizer Optimization for 10-Gb/s Data Transmission through Lossy Backplane

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Abstract—This paper proposes an optimization method for transmitter equalizers for high speed serial data transmission through lossy backplane channels. Detailed analytical analysis of transmitter equalizer design is carried out on the basis of variable tap spacing finite impulse response (FIR) filter. Results on a highly lossy 40-inch FR4 backplane channel are compared and discussed.

I. INTRODUCTION

According to theoretical analysis and measurements, the energy loss per unit length of backplane due to skin effect and dielectric loss increases almost exponentially with frequency [1]. In modern large communication systems both the data rate and the length of backplane increase. Therefore, the received signals become more and more distorted by the channel. Data and clock recovery (CDR) is not possible without proper equalization. FIR type transmitter equalizer or pre-emphasis because of its simplicity and suitability to implement in sub-micrometer CMOS integrated circuits is widely used in multi-gigahertz backplane transceivers. Historically pre-emphasis was implemented in data center oriented T-spaced FIR filter (called NRZ data equalizer hereafter), where T is 1 baud period. However, with the ever increasing data rate, the signal to noise ratio (SNR) at data centers and jitter at transition edges [2] of the received signals equalized by an NRZ data equalizer become worse and worse. A method to circumvent the problem is to reduce bandwidth. Bandwidth compression methods such as 4-level pulse amplitude modulation (PAM4) and duobinary were recently investigated [3–5]. Unlike PAM4 duobinary does not reduce the data rate of the transmission through backplane. Instead it takes the advantage of the natural roll-off of backplane. Compared with NRZ data equalizer, a problem associated with PAM4 and duobinary is the more complex clock and data recovery at receiver. Clock and data recovery scheme for duobinary is simpler than for PAM4. Even though the received signal still has three levels instead of two and clock recovery may fail when the input data is a 1-bit toggle data sequence [3]. We recently showed that this problem can be solved by using edge based equalizer proposed by Bruun [6]. We also showed that the amplitude of the target responses of edge equalizer and duobinary are identical but their phases are different [7].

Non-return-to-zero (NRZ) data equalizer, duobinary equalizer, and PAM4 equalizer are compared in [8]. Edge equalizer [6], equalizer that can suppress ISI at data centers and jitter at transition edges simultaneously [9], and equalizer whose FIR filter has variable tap spacing [10] are not discussed. In section II we introduce a general FIR pre-emphasis circuit with variable tap spacing. In section III we discuss the design and optimization of NRZ data equalizer and half-rate equalizer that suppresses ISI and jitter simultaneously on a highly lossy 40-inch FR4 backplane channel. Conclusion is made in section V.

II. A POPULAR FIR PRE-EMPHASIS CIRCUIT

Fig. 1 shows a popular FIR pre-emphasis circuit. The input binary data are delayed with variable tap spacing (Δ). The delayed data are held for 1 baud period (T). The equalizer FIR filter multiplies each tap with a tap coefficient Cn. All taps are added up at the output.

When the variable tap spacing is the baud period, the delay cells can be removed and the circuit becomes a conventional T-spaced FIR pre-emphasis equalizer. Fig. 2(a) shows an example of a 2-tap FIR TX equalizer implemented in sub-micrometer CMOS current mode logic (CML). The coefficient of the second tap is assumed to be negative so that its differential inputs are swapped. Fig. 2(b) shows a more programmable CML unit in which CtrP and CtrN are used to control the sign of a coefficient [11]. A first order estimation of the power consumption of an M-tap FIR TX equalizer is:

\[ P = V \cdot \sum_{n=0}^{M-1} \left| c_n \right| \]

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where $V_{DD}$ is power supply voltage, $I_n$ is bias current of the $n$th unit cell, $R$ is the load resistance, and $C_n$ is coefficient of the $n$th unit cell. In practice the power consumption is larger than what is predicted by equation (1) because it does not take into account the currents that flow into parasitic capacitors and the power consumed by control logic circuits. However, it is reasonable to use equation (1) to compare the power consumption of different equalization schemes with the same circuit structure when optimizing performance such as SNR at data centers or jitter at transition edges. In this paper the power constraint is a 0.5V voltage swing over a 50-ohm load resistor.

When the variable tap spacing is a half baud period (0.5T), the delay cells can also be removed and the circuit can be implemented in a half-rate structure which is shown in Fig. 3.

III. ANALYTICAL ANALYSIS AND MODELING

The output of a unit cell $b_n(t)$ in Fig. 1 can be expressed as:

$$b_n(t) = c(n) \cdot a(k) \cdot \text{rect}(t - kT - n\phi, T)$$

(2)

where $c(n)$ is the coefficient of the unit cell, $a(k)$ is the binary input, and $\text{rect}(t, T)$ is a rectangular function defined as:

$$\text{rect}(t, T) = \begin{cases} 1, & 0 < t < T \\ 0, & \text{otherwise} \end{cases}$$

(3)

In practice the baseband modulation waveform cannot have zero rise time or zero fall time. However, highly lossy backplane channels attenuate much the energy at very high frequencies. It turns out that $\text{rect}(t, T)$ is a very good approximation of practical baseband modulation waveform. The output of the transmitter $s(t)$ is the sum of the output of all taps and is expressed in equation (4).

$$s(t) = \sum_{n=0}^{N} b_n(t)$$

(4)

This signal is sent to backplane and the output at the receiver end is

$$r(t) = s(t) * m(t) = a(k) \sum_{n=0}^{N} c(n) \cdot \text{rect}(t - kT - n\phi, T) * m(t)$$

(5)

where $m(t)$ is impulse response of the backplane channel, $*$ is the convolution operator. We define a pulse response of the channel as $h(t)$.

$$h(t) = \text{rect}(t, T) * m(t)$$

(6)

Applying the superposition theorem to the backplane we get the final expression of the received signal $r(t)$ as

$$r(t) = \sum_{k=-\infty}^{\infty} r_k(t) = \sum_{k=-\infty}^{\infty} a(k)c(n)h(t - kT - n\phi)$$

(7)

The received signal is a continuous time analog signal. We usually need to sample the received signal at data centers and transition edges to recover clock and data. Successful clock and data recovery must have sufficient SNR at data centers and sufficient timing information at transition edges [12]. When the input data is a Kronecker delta, only some pre-defined waveforms can achieve this target. The waveforms are called target responses.

For NRZ data equalizer and PAM4 equalizer, the waveform of target response is a Kronecker delta. For duobinary and edge equalizer the target response is $(I - i z^r)$. In fact target response is the sampled version of the received signal when the input is a Kronecker delta. Fig. 4 shows typical timing for the input pulse, channel pulse response, and target response of a virtual equalizer.

$$y(m) = r(m \zeta + \tau) = \sum_{k=-\infty}^{\infty} \sum_{n=0}^{N} c(n) h(m \zeta + \tau - kT - n\phi)$$

(8)

where $m$ is an integer, $\zeta$ is time interval to sample the received signal, and $\tau$ is the delay shown in Fig. 4. We can conclude from equation (8) that we have 4 dimensions of freedom when designing a transmitter equalizer’s coefficients $\{C_n\}$. They are $y(m)$, $\zeta$, $\tau$, and $\phi$. This observation, to our best knowledge was not discussed in literature. The time interval $\zeta$ can only take discrete values. When it is 2T, the target response should be zero-forcing PAM4 equalization; when it is T, the target response can be zero-forcing NRZ data equalization or duobinary equalization or edge equalization. When it is 0.5T, the target response is able to minimize ISI at data centers and jitter at transition edges simultaneously.
IV. EQUALIZER OPTIMIZATION

The freedom to choose the 4 parameters in equation (8) allows us to optimize FIR transmitter equalizers. The sampling time interval $\zeta$ and target response usually serve specific purposes. Variable tap spacing $\phi$ other than 0.5T and 1T usually makes the circuit complex. Therefore, the most frequently used parameter for optimization is $\tau$.

It can be inferred from equation (1) that if two sets of coefficients $\{C_n\}$ are derived for a given target response, the set whose absolute sum is smaller consumes less power or has a larger vertical eye opening for a given power. This provides a guideline for FIR TX equalizer optimization. The simplest way to do it is to sweep the delay time $\tau$ to find the minimum of the absolute sum of filter coefficients. Since $\tau_1$ is fixed, what we need to do is to sweep $\tau_2$.

Design and optimization examples are carried out on 10-Gb/s data transmission through a practical 40-inch backplane on FIR4. The channel is named B20 on the IEEE 802.3ap public website [13]. It has a 20-inch trace and two 10-inch line card. The attenuation factor is about -4dB/GHz. We only compare a 10-tap NRZ data equalizer and a 10-tap half-rate equalizer that can suppress ISI at data centers and jitter at transition edges simultaneously. We can use frequency domain methods for the two cases. Although time-domain solutions based on equation (8) can give the value of filter coefficients. It is well-known to designers that the results are sensitive to sampling instants and target responses at sampling instants outside the watching window are not guaranteed. Although frequency domain methods may not outperform time domain methods if the number of coefficients is very few, they generally yield better performance when the number of coefficients increases. In addition, they bring more insight for designers. The frequency domain method used to derive filter coefficients is given in equation (9) for $\zeta$=1T and equation (10) for $\zeta$=0.5T [14].

$$C(aT) = T \cdot R(aT) \cdot \exp(-jaT) \left[ \sum_{-\infty}^{\infty} H(a - 2kn_1) \cdot \exp(-jkw_0) \right]^{-1}$$ (9)

$$C(aT) = T \cdot R(aT) \cdot \exp(-jaT) \left[ \sum_{-\infty}^{\infty} H(a - 2kn_1) \cdot \exp(-jkw_0) \right]^{-1}$$ (10)

where $R$ is the target response, and $w_0$ is angular frequency at baud rate.

Fig. 6. Eyediagram of received signal unequalized.

Fig. 7. Eyediagram of received signal equalized by a NRZ data equalizer ($\tau_2$=0.89T).

Fig. 8. Eyediagram of received signal equalized by a NRZ data equalizer ($\tau_2$=0.3T).

Fig. 5 compares the sum of the modulus of filter coefficients for a half-rate (solid), a full-rate (dotted) and a conventional NRZ data equalizer (dashed). The full-rate
equalizer is discussed in [5] and needs much more complicated circuit than what is shown in Fig. 1. The relative offset is defined as the displacement from the peak of the equalized pulse response to the peak of the un-equalized pulse response, which is shown in Fig. 1 as $\tau_2$. The large variation of the sum shows that there is big difference of the equalized vertical eye opening when different set of coefficients are used. In a real circuit there is only finite number of taps and each tap has a finite resolution. The difference may become much larger.

Fig. 6 shows the eyediagram of the un-equalized signal at the far end. Fig. 7 shows the eyediagram of the equalized signal with a NRZ data equalizer whose $\tau_2$ is 0.89T. It is not possible to give a clean eyediagram when $\tau_2$ is 0.39T which corresponds to the peak shown in Fig. 5. Instead we draw the eyediagram of the equalized signal with a NRZ data equalizer whose $\tau_2$ is 0.3T in Fig. 8. Fig. 9 and Fig.10 show the eyediagrams of the received signal equalized by a half-rate equalizer that can suppress ISI and jitter simultaneously. Fig. 9 has $\tau_2$ of 0.38T and Fig. 10 has a $\tau_2$ of 0.18T. For both equalizers, the optimized eyediagram has much larger vertical opening and horizontal eye opening than that of an un-optimized equalizer. The results demonstrate that changing $\tau_2$ can optimize system performance.

V. CONCLUSION

We propose an optimization method for transmitter equalizers for high speed serial data transmission through lossy backplane channels. A general analytical model which is valid for many types of transmitter FIR equalizer design is presented. Results on a practical 40-inch FR4 backplane verify our model and optimization methods.

REFERENCES


