A 0.18–µm CMOS Receiver with Decision-feedback Equalization for Backplane Applications

Abstract—Decision-feedback equalization (DFE) is explored to reduce inter-symbol interference (ISI) and crosstalks in high-speed backplane applications. In the design of clock and data recovery (CDR) circuit, embedding DFE within phase and frequency detector (PFD) enhances to recover data inherently from distorted input signals and facilitates to provide DFE with recovered clock. With PRBS15 data signaling at 5-Gb/s over 34” FR4 backplane, SPECTRE simulation in 0.18-µm CMOS process has shown the design feasibility.

I. INTRODUCTION

The speed of serial links across copper backplanes has seen a steady rise over the past few years. As data rates increase, transmission suffers from severe eye closure caused by ISI due to high frequency attenuation of the copper traces drawn on PCBs, crosstalk noise between connector pins, and reflections that occur as data rates move into the microwave frequency range of operation and beyond. To enable reliable operation on dispersive channels at a given Baud rate, the I/O architecture can employ some form of line equalization techniques. The feed-forward equalization (FFE) comprises of a discrete-time FIR filter and continuous-time analog equalizer. When used as pre-emphasis at transmit (TX), FIR filter pre-distorts the signal such that it is recovered at the receive (RX) side with a desired shape suitable for reliable data detection. The analog equalizer is realized by summing the outputs of a DC path and an AC path, which is a differential pair degenerated by an RC network. The response of the analog equalizer is optimized to match the high-frequency roll-off of a backplane trace. The above equalization techniques are effective in counteracting ISI but unsuitable for some legacy backplanes with significant high-frequency crosstalk since they amplify high-frequency noise. PAM-4 alternatives alleviate ISI but have interoperability issues and suffer from reduced voltage margins that exacerbate crosstalk effects.

Another form of equalization is the decision-feedback equalization, or DFE [1-5], which can overcome the drawback of high-frequency noise amplification. DFE uses clean decisions of previously received symbols to remove ISI in the current symbol. Since it does not boost high-frequency noise such as crosstalk or wideband noise to equalize the channel, this technique can be suitable for backplane environments with high channel count.

At RX clock signal is needed for delaying the currently received data to obtain prior data decision. In [2], a PLL block is used to generate multiphase clocks. The RX uses the PLL clock as an initial guess for the incoming data phase and frequency. The exact phase and frequency at the RX is recovered from the data by a digital clock and data recovery loop architecture. In [3], the FFE without the DFE opens the input data eye enough to permit the CDR to achieve lock and thus obtain the clock information for DFE later operation. In [4], the CDR is also parallel to DFE. A PLL with reference clock is needed for CDR operation. With serial loop-back, the clock signals are obtained by CDR and then provided for DFE operation. In this paper, the DFE circuit is embedded in the PFD design of the CDR circuit, enabling clock recovery and DFE operation concurrently. The link architecture is shown in Fig. 1.

Look-ahead DFE (LADFE) structure with only one post-tap is employed in [4, 5]. Although maximum data rate can be obtained with LADFE due to its smallest loop feedback delay, the hardware overhead, like in [2], may become prohibitive when a large number of taps is required for legacy backplane system. In this paper, a multi-tap half-rate DFE structure is used. In 0.18-µm CMOS technology, SPECTRE simulation shows the clock and data recovery at RX after PRBS15 data transmit over a typical 34” FR4 backplane at 5-Gb/s. Without other equalization techniques applied, only a 2 post-tap DFE is used to remove ISI for such system. For higher data rates or some legacy system, DFE can be complemented with FFE.

Section II presents the DFE structure. CDR circuit design is given in Section III. Section IV shows the simulation results. Finally Section V gives conclusions.
II. DFE STRUCTURE

Based on DFE structure in [1], the proposed 2 post-tap DFE structure with half-rate clock timing is shown in Fig. 2.

![Figure 2. 2 post-taps DFE structure](image)

The DFE comprises of odd and even branches. Each branch consists of a FIR filter equalizer (EQ), followed by two D flip-flops (DFFs). The outputs of the first DFFs are fed to the opposite branch to provide the first feedback post-tap to EQ in each branch. The second DFF in each branch is triggered with clock edge opposite to that used for the first DFF. Its output goes directly to the EQ in the same branch to form the second post-tap. The outputs of odd/even branches are serialized by a 2:1 multiplexer (MUX) to obtain the full-rate data. The DFE in [1] has only one post-tap. At higher speed or for more legacy backplane, multi-tap DFE is required to counteract the increasing post-cursor ISI of the backplane channel. The structure in Fig. 2 can be easily extended to multi-taps by adding more DFFs with interleaved clock triggering. The DFE component circuits are designed in current-mode logic (CML), and their implementations are shown in Fig. 3.

![Figure 3. Implementations of (a) EQ; (b) D latch; (c) MUX.](image)

Fig. 4 shows the timing analysis of the 2 post-tap DFE structure in Fig. 2. Suppose the current input data to DFE (IN0 to EQ) is data 8, the previous two data inputs (IN1 and IN2 to EQ) should be data 7 and data 6. It can be seen that data 7 is from the first DFF of odd branch in Fig. 4(a) and data 6 is from the second DFF of even branch in Fig. 4(a). It can be further observed that the transition of one-symbol delayed data (IN1) is aligned with the transition of two-symbol delayed data (IN2). Then adding more post-taps has no effect in increasing the feedback loop delay, which is defined by

\[ T_{\text{delay}} = T_{\text{eq}} + T_{\text{samp}} + T_{\text{cq}} \]  

where \( T_{\text{delay}} \) is the total feedback loop delay, \( T_{\text{eq}} \) is the FIR equalizer delay, \( T_{\text{samp}} \) is the clock-to-data time, and \( T_{\text{cq}} \) is the clock-to-output delay. In order for the immediate previous data (data 7) not to lag the current data (data 8), \( T_{\text{delay}} \) should satisfy the following equation

\[ T_{\text{delay}} \leq T_{\text{symbol}} \]  

For the best eye sampling, \( T_{\text{samp}} = T_{\text{symbol}} / 2 \), then the maximum data rate is determined by

\[ f_{\text{max}} = \frac{1}{2(T_{\text{eq}} + T_{\text{samp}})} \]

![Figure 4. Timing analysis of (a) odd branch and (b) even branch](image)

III. CDR DESIGN

In this paper the half-rate bang-bang PFD structure proposed in [6] is employed, with the double-edge-triggered
flip-flop (DETFF) replaced by the DFE structure in Fig. 2.

Fig. 5 shows the PFD structure with DFE embedded.

![Figure 5. PFD structure with DFE embedded](image_url)

Fig. 6(a) shows the architecture of the CDR circuit. The FLL consists of FD, comparator (COMP), charge pump (CP), low-pass filter (LPF) and VCO. The PLL consists of PD, COMP, CP, LPF and VCO. The FLL and PLL share the same VCO. A switching circuit, shown in Fig. 6(b), assists the transition from the coarse control to the fine control. It consists of two AB+CD logic circuits and a transmission gate (TG). Its inputs come from comparator outputs in the coarse FLL. The outputs control the fine PLL. Fig. 7 shows the implementations of COMP and CP.

![Figure 6. (a) Proposed CDR architecture. (b) Switching circuit.](image_url)

![Figure 7. (a) Comparator. (b) Charge pump.](image_url)

Table I gives the outputs of AB+CD logic circuits with the values of A, B, C and D set by the FLL lock conditions. The outputs of AB+CD (I) and AB+CD (II) are differential, controlling the TG. The inputs to TG are connected to a reference, which is set to the common-mode voltage of the fine VCO control. For frequency-out-of-lock cases (Case #1 and Case #2), the TG connects VCO fine controls to the common-mode voltage to ensure that VCO fine control voltage falls within the linear frequency region. A large deviation voltage of fine control lines may introduce slewing in the PLL after the FLL is locked, potentially causing the PLL to become unlocked. At frequency-locked state, which is Case #3, the TG is open and the PLL starts to fully take control to prevent false locking.

<table>
<thead>
<tr>
<th>Case</th>
<th>A (I/II)</th>
<th>B (I/II)</th>
<th>C (I/II)</th>
<th>D (I/II)</th>
<th>AB+CD</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0/0</td>
<td>1/0</td>
<td>1/1</td>
<td>0/1</td>
<td>0 (I)/1 (II)</td>
</tr>
<tr>
<td>2</td>
<td>1/1</td>
<td>0/1</td>
<td>0/0</td>
<td>1/0</td>
<td>0 (I)/0 (II)</td>
</tr>
<tr>
<td>3</td>
<td>1/1</td>
<td>1/0</td>
<td>0/0</td>
<td>0/1</td>
<td>1 (I)/0 (II)</td>
</tr>
</tbody>
</table>

A four-stage ring oscillator is shown in Fig. 8(a). The implementation of each stage is shown in Fig. 8(b). A MUX is introduced in our design to create low band and high band for tuning range extension. The VCO controls are decomposed into coarse/fine inputs (Vcoar/Vfin). The coarse/fine steering currents (Icoar/Ifin) are cross-coupled and Icoar is designed to be an order higher than Ifin.

![Figure 8. (a) Four-stage ring oscillator. (b) Single stage implementation.](image_url)

IV. SIMULATION RESULTS

PRBS15 data is transmitted at 5-Gb/s over a typical 34" FR4 backplane system (30" trace and 2*2" connectors), which has 15dB attenuation at 2.5GHz. The backplane system characteristics are based on measured s-parameters. Only a 2 post-tap DFE (Fig. 2) is employed as equalization. In 0.18-µm CMOS process, SPECTRE simulation shows the following results. The coarse/fine inputs to VCO show their
convergences in Fig. 9. In CDR lock condition, CLK0 aligns with the edge of input data. Thus CLK90 samples the data at its eye center. Fig. 10(a) shows the eye diagram of the input data at far-end of backplane system, compared with the recovered data eye diagram with CLK90 timing in Fig. 10(b).

![Figure 9. Convergence of VCO control inputs: TOP – fine control, BOTTOM – coarse control](image)

(a) (b)

Figure 10. (a) Eye diagram of input data to CDR; (b) eye diagram of recovered data

Fig. 11 shows the recovered clock in the time and frequency domain. It is read that the peak-to-peak jitter of the recovered clock is about 0.06UI. Fig. 12 shows the eye diagrams at the outputs of EQs at even and odd branches inside DFE in Fig. 5. It is observed that the eyes are opened and closed alternatively, corresponding to those shown in timing analysis (Fig. 4).

![Figure 11. (a) Recovered clock in time domain; (b) power spectrum of recovered clock](image)

(a) (b)

V. CONCLUSIONS

The core circuits of a 0.18-µm CMOS backplane receiver are designed. Decision-feedback equalization is explored and embedded in the design of clock and data recovery circuit. SPECTRE simulation exhibits a recovered clock with peak-to-peak jitter of 0.06UI after RBS15 data transmits over a 34” FR4 backplane at 5-Gb/s. The core circuit power consumption is 60mW at a 1.8V supply.

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REFERENCES


