A 40-GHz Frequency Divider in 90-nm CMOS Technology

Muhammad Usama and Tad. A. Kwasniewski
Department of Electronics, Carleton University
1125 Colonel By Drive, Ottawa ON, K1S 5B6 Canada.
{musama, tak}@doe.carleton.ca

Abstract—This paper presents the design of a high-speed wide-band frequency divider. The divider core is formed with a low voltage swing current mode logic (CML) structure, which enables high frequency operation at very low power dissipation. The divider exhibits very wide locking range from 4GHz - 41GHz, and it has an input sensitivity of -31dBm at 30GHz. The divider core draws only 750µA from a 1.2V supply. Post layout simulation results in 90-nm CMOS technology are provided.

I. INTRODUCTION

Frequency dividers are used in many communications applications such as frequency synthesizers, timing-recovery circuits, and clock generation circuits. In a phase locked loop (PLL) a frequency divider is employed within the loop to divide down the local oscillator frequency and to provide the programmability of the synthesizer. Frequency divider is one of the most critical blocks of the system because it operates at the highest frequency. In particular, the power reduction of the frequency divider in the first stage is effective in realizing a low-power PLL. This is the key point for the high-speed operation and low power consumption. The phase noise generated by the divider can affect the synthesizer noise performance within the PLL band, especially if a high division factor is used. In fact, the divider noise power is multiplied by the square of the division factor, when it is transferred to the PLL output [1].

Digital frequency dividers are the most popular divider structures in use today. They offer divider ratio programmability, higher division ratios and easier digital control. The fundamental element of a digital frequency divider is a D-type flip-flop, or two level-sensitive latches in a master-slave configuration [2]. These dividers achieve a broader bandwidth than other types of dividers in low to medium range of frequencies. High-speed digital frequency dividers are typically implemented using the current mode logic (CML) latches. The CML latches exhibit better performance than other clocked storage elements. Large frequency ranges are not therefore uncommon in these dividers that use CML style [12].

With the aggressive scaling of CMOS transistors, multi-gigahertz dividers are now realizable in CMOS technologies. Several high-speed frequency dividers in modern CMOS technologies have been reported in recent publications [6]-[11], [13], and [14].

This paper presents the design of a CML based frequency divider in a state-of-the-art 90-nm CMOS technology. The presented divider achieves not only a very high operating frequency but reasonably low power dissipation. The divider structure and its operation are described in Section-II. Post layout simulation results in 90-nm CMOS technology are also provider in Section-III along with a comparison of the presented divider with other recently published results.

II. DIVIDER STRUCTURE

Conventionally for a divider application, two identical CML latches are used in a master-slave configuration as shown in Fig. 1. Because of the parasitic capacitance of the transistors of sample circuit, the tail current must be sufficiently high to achieve a wider range of linearity, a higher slew rate and a larger transconducance. On the other hand the hold circuit does not need such a large bias current. These conflicting requirements can not be reconciled in conventional CML latch design because they have only a single constant current source.

It is possible to simplify the usual CML latch clocking structure by employing a single clock transistor pair to switch the current between the sample and hold pair of the master and slave latches [2]. This new configuration uses a single bias
current source for both latches. Schematic diagram of the modified CML divider is shown in Fig. 2. In the master-slave combined latch technique [2], the sample/hold current difference is accomplished by using smaller transistor sizes for the hold pairs of both latches. This can be used to make most of the current flow through the sample pairs. Due to the lower current through hold pair the width of the current source does not need to be doubled – a 1.5 times transistor width for the current source is sufficient for successful operation at the same operating frequency. This reduces the overall static power dissipation. This technique is also area efficient, because the current source is the dominant area-occupying component (if active loads are used). Using single current source and clock transistors, can save up to 20% of the layout area. Small transistor sizes offer lower diffusion capacitance at the output terminals, which results in lower D-Q delay and higher operating frequency.

III. SIMULATION RESULTS

Post layout simulations were conducted for the frequency divider implemented in STM’s 90-nm CMOS technology, with Spectre as the simulator. Simulations were done in a nominal process corner at 27°C temperature. The supply voltage used was 1.2V and the small signal swing is set to be 400mV. The time domain waveforms of the input and the output signals at 40-GHz frequency are shown in Fig. 3. A sinusoidal input is used. Small distortion can be seen at the output, but the signal swing is adequate to drive subsequent divider stages.

The divider operates in a very wide frequency range from 4GHz to 41 GHz, achieving a 37GHz locking range, as shown in Fig. 4. Due to constant current flow, the power consumption is almost flat over the frequency range. The divider core draws only 750µA from the 1.2V supply, dissipating less than 1mW of power.

The input sensitivity is another very important parameter characterizing RF frequency range of the divider. It is the minimum power of the input signal necessary for a proper divider operation as a function of frequency. A data set depicting the input sensitivity of the divider is plotted in Fig. 5. The divider achieves the highest input sensitivity of -31dBm (~8mV in a 50Ω system) at 30GHz.

![Fig. 2. High frequency CML divider core structure [2].](image1)

![Fig. 3. Input and output waveforms of the divider at 40GHz frequency.](image2)

![Fig. 4. Average current and locking range of the divider.](image3)
This structure combines two conventional level CML latches. The divider core comprised of a low swing CML structure. A frequency divider in 90-nm CMOS technology is presented. It can be seen that the divider in [3] has by far the best FOM. Amongst the high frequency dividers the presented structure is one of the best for high frequency and low power operation. The presented frequency divider is particularly suited for ultra-wideband, low-power applications.

**ACKNOWLEDGMENT**

The authors would like to thank Altera Corporation, Communication and Information Technology Ontario (CITO) and Natural Sciences and Engineering Research Council (NSERC) for their generous support. Technology access from Canadian Microelectronic Corporation (CMC) is also appreciated.

**TABLE I**

Comparison with other published results

<table>
<thead>
<tr>
<th>Reference</th>
<th>CMOS Tech.</th>
<th>FMAX [GHz]</th>
<th>PDISP [mW]</th>
<th>FOM</th>
<th>Locking Range [GHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[4]</td>
<td>0.18µm</td>
<td>2.2</td>
<td>14.4</td>
<td>0.2</td>
<td>----</td>
</tr>
<tr>
<td>[3]</td>
<td>0.2µm</td>
<td>4.3</td>
<td>0.044</td>
<td>97.7</td>
<td>2.3</td>
</tr>
<tr>
<td>[5]</td>
<td>0.35µm</td>
<td>5.2</td>
<td>2.5</td>
<td>2.1</td>
<td>4.2</td>
</tr>
<tr>
<td>[6]</td>
<td>0.18µm</td>
<td>10</td>
<td>1.3</td>
<td>7.7</td>
<td>5</td>
</tr>
<tr>
<td>[7]</td>
<td>0.13µm</td>
<td>15</td>
<td>3.6</td>
<td>4.2</td>
<td>4</td>
</tr>
<tr>
<td>[8]</td>
<td>0.18µm</td>
<td>18</td>
<td>1.3</td>
<td>13.8</td>
<td>16.5</td>
</tr>
<tr>
<td>[9]</td>
<td>0.18µm</td>
<td>18</td>
<td>7.2</td>
<td>2.5</td>
<td>16</td>
</tr>
<tr>
<td>[10]</td>
<td>0.13µm</td>
<td>20</td>
<td>12.5</td>
<td>1.6</td>
<td>----</td>
</tr>
<tr>
<td>[11]</td>
<td>0.13µm</td>
<td>38</td>
<td>12</td>
<td>3.2</td>
<td>3.5</td>
</tr>
<tr>
<td>[12]</td>
<td>0.18µm*</td>
<td>40</td>
<td>9</td>
<td>4.4</td>
<td>----</td>
</tr>
<tr>
<td>[13]</td>
<td>0.18µm</td>
<td>40</td>
<td>31</td>
<td>1.3</td>
<td>2.3</td>
</tr>
<tr>
<td>[14]</td>
<td>90nm</td>
<td>44</td>
<td>5.3</td>
<td>8.3</td>
<td>40</td>
</tr>
<tr>
<td>This work</td>
<td>90nm</td>
<td>41</td>
<td>0.9</td>
<td>40.0</td>
<td>37</td>
</tr>
</tbody>
</table>

* BiCMOS Process

**REFERENCES**


