An Eye Detection Technique for Clock and Data Recovery Applications

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Abstract -- An eye detection technique to detect maximum vertical eye opening points for data recovery circuit (CDR) applications and the circuit implementation of an eye detector (ED) are reported in this paper. The ED samples the incoming data to generate the retimed data and produces an error signal indicating whether the sampling point leads or lags the maximum eye opening point, where the lowest BER is expected. The ED is implemented in CMOS 0.18μm technology, and its feasibility is confirmed by transistor-level simulations.

I. INTRODUCTION

In data communication systems, the clock and data recovery circuit, which extracts the timing information from the incoming data and provides retimed data and the corresponding clock for the following blocks, is the key building block, and its performance significantly affects on the quality of a serial data link. There are many CDRs reported in the literature [1-4] and almost all of them are based on transition edge detection, i.e. the recovered clock is extracted from the timing information of data transition edges. In those approaches, the incoming data is normally sampled at the middle point of two adjacent potential transition edges regardless of the shape of the incoming eye diagram. In [4], the edge distribution possibility is considered, but not the shape of the opened eye. A multiple-phase VCO is normally required in edge-detection CDRs to provide multiple-phase clocks for phase/frequency detection and data sampling. A symmetric eye diagram is assumed for those CDRs, while the eye diagram of the incoming data is normally asymmetric, depending on the data source, transmission channel, receiving buffer and so on. Obviously the optimum data sampling points to achieve the lowest bit-error-rate (BER) is where the data eye opens the widest, say, maximum eye opening points. In this paper, an eye-detection technique is proposed, by which a novel clock and data recovery mechanism, utilizing the timing information of the incoming data’s maximum eye-opening points, can be implemented. It is a binary eye-detection technique, by which zeros or ones are produced depending on whether the clock edges lead or lag the maximum eye opening points. The output can be used to tune a clock generator to realize the data and clock recovery, so that the incoming data is sampled at the maximum eye-opening points and the lowest BER is expected. Furthermore, because only one clock signal is required for the eye-detection, the clock generator can be far simpler than those of traditional CDRs, e.g. a commonly used single-stage LC oscillator can be employed as well.

II. PRINCIPLE OF THE EYE DETECTION

The concept of the eye detection is shown in Fig. 1. The eye diagram of the incoming data (Din) is illustrated in the upper-left of the figure, and some possible sampling points (triggered by the edges of ClkIn) are also indicated in the figure. The eye detector samples the incoming data and produces the output data (Dout). In the mean time, an error signal (Err) is produced according to the relative position of actual sampling point comparing to the maximum eye opening point. As shown in the figure, the error output is “1” when the sampling point leads the maximum eye opening point, otherwise, the error output is “0”. Because the data sampling is achieved inherently in the eye detection, there is no phase mismatch problem between clocks for the detector and for the actual data sampler.

The eye detector produces the error signals in two steps. Firstly, it measures the level of the eye opening at a certain sampling point, then it determines if the sampling point leads or lags the maximum eye opening point. The schematic of the proposed eye detector is shown in Fig. 2. The incoming data is sampled by three Variable-threshold Double-edge-triggered Flip-Flops (VtDetFFs). The VtDetFF1 and VtDetFF2 are triggered by the same clock (ClkIn) while the clock for VtDetFF3 is the delayed version of ClkIn, with the delay of approximately one-tenth of the symbol period. The outputs of the VtDetFF1 and VtDetFF2 are compared to simultaneously adjust the threshold voltages of VtDetFF1 and VtDetFF3 with a charge pump (CP), in other words, the threshold voltage is decreased if the two outputs are different, otherwise the threshold voltage is increased. The threshold voltage of

![Figure 1. The concept of the eye diagram](image-url)
VtDetFF2 is fixed at zero and its output is the retimed data. The error signal of the eye detector is generated by comparing the outputs of VtDetFF1 and VtDetFF3.

A critical component of the eye detector is the VtDetFF, whose threshold voltage is tunable. The symbol of the VtDetFF is shown in the left side of Fig. 3, in which all signals except for $V_{ct}$ are differential. A commonly used DetFF samples the input ($V_{in}$) at the clock edges and the output ($V_{out}$) is determined by the sign of the input at the clock edges, i.e. the input threshold voltage is zero. In a VtDetFF, this threshold voltage is tuned by the control signal $V_{ct}$. The threshold voltage is zero and the VtDetFF operates exactly the same as a DetFF when $V_{ct}$ is zero. By increasing $V_{ct}$, the threshold voltage ($V_{th}$) is increased and the relation between $V_{out}$ and $V_{in}$ is shown in the right side of Fig. 3. It is notable that the VtDetFF has a memory effect with respect to the signal $V_{in}$. The actual threshold voltage is $V_{th}$ when $V_{in}$ increases and $-V_{th}$ when $V_{in}$ decreases. As a result, a window with a width of twice of $V_{th}$ is created as shown in Fig. 3. It is a desired feature for the eye detector because this window is to fit the eye opening of the incoming data by a threshold voltage adjustment loop in the eye detector.

The operating principle of the threshold voltage adjustment loop is illustrated in Fig. 4, in which $I$, $II$ represent the sampling positions and the threshold voltages of VtDetFF1, VtDetFF2 respectively. The height of $I$ corresponds to the voltage difference of $2*V_{th}$ as the width of the window shown in the right side of Fig. 3. In Fig. 4A, the threshold voltage is smaller than the eye opening at the sampling point.

\[ V_{in} \rightarrow \text{VtDetFF} \rightarrow V_{out} \]

\[ V_{in} \leftarrow \text{VtDetFF} \rightarrow V_{out} \]

Figure 3. Characteristics of the VtDetFF

![Figure 2. The schematic of the eye detector](image)

![Figure 4. Operating principle of the threshold voltage adjustment loop](image)

![Figure 5. Operating principle of the error signal production](image)
sent the sampling points and threshold voltages for \( V_{\text{tDetFF}1} \), \( V_{\text{tDetFF}2} \) and \( V_{\text{tDetFF}3} \) respectively. In Fig. 5A, the sampling point leads the MEO, and in Fig. 5B, it lags the MEO. Because I and III have the same height, one can say that the sampling point leads the MEO (as case A in the figure) if Q1 is different from Q3, where Q1, Q2, Q3 are outputs of \( V_{\text{tDetFF}1} \), \( V_{\text{tDetFF}2} \), \( V_{\text{tDetFF}3} \) respectively. If Q1 is always the same as Q3, one can say that the sampling point lags the MEO (as case B in the figure).

Both the internal charge pump and the one to be attached to the output of the eye detector have asymmetric structure, i.e. discharging and charging currents are not equal, the current ratios mainly depend on the transition probability of the incoming data and the jitter performance specification. Some techniques can be employed so that those current ratios can be independent of the data transition probability. Details on this issue are not given in this paper due to the space constraints.

III. CIRCUIT IMPLEMENTATION

A. Variable-threshold double-edge-triggered flip-flops

According to the operating principle discussed above, the \( V_{\text{tDetFF}} \) is an important building block in the eye detector. A widely used DetFF is shown in Fig. 6. There are two D Latches which latch the data at the high and low levels of the clock respectively, and their outputs (latched values only) are selected by a multiplexer according to the clock signal to produce the output of the DetFF.

The schematic of the D latch used in this type of DetFF is shown in the right side of the figure, in which a current source (\( I_{\text{bias}} \)) is fully steered to two differential pairs (I1 and I2) alternatively by the clock signal. The current I1 is for the input stage which is controlled by the input data. I2 is the bias current for another differential pair, connected in a positive feedback mode for the latching propose. Fig. 7A illustrates the relation between I1/I2 and \( V_{\text{clk}} \). To achieve a hysteresis and a tunable threshold required for a \( V_{\text{tDetFF}} \), the current I1 and I2 are set as shown in Fig. 7B. When the current is steered to the input stage, a certain amount of current

\[
I_{\text{res}} \quad I_{\text{bias}} - I_{\text{res}}
\]

is maintained for I2 so that the latching pair still partially functions when the input stage is activated. As a result, the threshold voltage is not zero, but a value related to \( I_{\text{res}} \). In this design, \( I_{\text{res}} \) is controlled by a tuning voltage \( V_{\text{ct}} \), so that a tunable threshold voltage can be achieved. The schematic of the control part of a \( V_{\text{tDetFF}} \) is shown in Fig. 8. A current (\( I_{\text{res}} \), controlled by the signal \( V_{\text{ct}} \)) is added to I2 while the same amount of current is subtracted from I1. During the pass through cycle, the current for the input stage is \( I_{\text{bias}} - I_{\text{res}} \) and the current for the latching stage is \( I_{\text{res}} \).

B. Charge pump for the threshold voltage adjustment

The internal charge pump adjusts \( V_{\text{ct}} \) according to the signal coming from the voltage threshold detection circuit. The threshold voltage is dynamically tuned in order to keep equal to the eye opening portion of the incoming data. Whenever a voltage difference between Q1 and Q2 is detected, the output of the corresponding XOR gate becomes high and the \( V_{\text{ct}} \) should be decreased, otherwise, \( V_{\text{ct}} \) should be increased. A simplified schematic of the charge pump is shown in Fig. 9.

IV. SIMULATION RESULTS

To confirm the feasibility of the proposed eye detection technique, an eye detector was implemented in CMOS 0.18µm technology, and simulated in the transistor-level with the testbench shown in Fig. 10, in which all signals in the data and clock paths are fully differential. In the testbench, a charge pump/loop filter (CP/LF) is driven by the error output
(Err_out) of the eye detector to tune the delay of a voltage-controlled delay cell (VCDC), and in this way the clock phase can be tuned. Once the loop achieves lock, the data sampler inside the eye detector is expected to sample the incoming data at the maximum eye opening points. The input data rate is set at 4Gb/s, and the input clock frequency is 2GHz (for half-rate operation).

A transient analysis was done to illustrate the locking process. The threshold control voltage (Vt) inside the eye detector and the VCDC tuning signal (Delay_Ctrl) are shown in Fig. 11. The tuning process of the Vct can be observed clearly for the first 100ns. Once the Vct is stable, the eye detector produces a signal Err out to tune the signal Delay Ctrl with the aid of a CP/LF. After 600ns, both Vct and Delay Ctrl are in lock.

Fig. 12 shows the eye diagram of the data and the clock when the loop is in lock. It is important that the data and clock are evaluated at the data sampler (VtDetFF2) inside the eye detector so that the sampling positions can be observed precisely. From Fig. 12, one can see that the zero-crossing points of the clock are exactly aligned to the maximum vertical eye opening points of the data.

V. CONCLUSIONS

This paper reports a novel technique to detect the maximum vertical eye opening points for clock and data applications as well as its CMOS circuit implementation, followed by its transistor-level simulation results. With this technique, a clock and data recovery circuit is able to locate the actual data sampling point where the eye diagram of the data opens widest so that the lowest BER can be achieved. In addition, the clock generator of a CDR employing this eye detector can be simplified because multiple phases are not necessary.

References


