METASTABILITY ANALYSIS OF CMOS CURRENT MODE LOGIC LATCHES

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Abstract

This paper presents a detailed analysis of metastable behavior in CMOS Current Mode Logic (CML) latches. The variation of the latch delay is primarily caused by the finite current transition time, which in fact depends on the rise/fall times of the clock signal. In this analysis a relation is defined between the latch characteristic parameters and the signal slew rates. The presented analysis is specific for CML latches, but it still gives insight of such behavior in other latch and flip-flop structures. 0.18\textmu m CMOS technology examples are provided.

Keywords: Metastability analysis, CMOS Current Mode Logic, CML Latches, signal slew-rate.

1. Introduction

A latch is a level-sensitive clocked storage element. It usually contains clock (CLK), data (D) as an input and an output (Q). During one phase of the clock the latch is transparent, this phase is called a transparent phase. The other clock phase is known as a latching phase, during which the output holds the previous data value and is not affected by any change at the data input. The clock edge between the transparent and the latching phase is called the isolating or triggering edge. The timing parameters for the latch are defined with respect to this triggering edge. Setup time is the minimum time the data can change before the triggering edge of the clock, such that a correct output value is produced. Hold time is the minimum time the data can change after the triggering edge of the clock.

The failure of a latch due to setup and hold time violations is not an abrupt process [1]. During the transparent phase of the clock, there is a certain delay between the last change in the data and the corresponding change at the output, denoted by $T_{DQ}$. This delay is not always constant; it depends on the relative position of the data with respect to the triggering edge of the clock, denoted by $T_{DC}$. For smaller $T_{DC}$, an increase in the $T_{DQ}$ can be seen before the latch fails to capture the data. Setup and hold times can be defined as the $T_{DC}$ time at which the latch delay $T_{DQ}$ increases by a certain amount (usually an arbitrary number around 5% to 10%) from its stable value [1].

This variation in the delay is due to the metastable behavior of the latch. Fig. 1 illustrates the regions of stability in the latch. A similar curve can be obtained for negative $T_{DC}$, showing the hold time.

This delay variation directly translates into jitter when these latches are used in circuits, like frequency prescalers. The main cause of metastable behavior is the finite rise/fall time of the clock and data. At multi-gigahertz frequencies the rise/fall times of these signals are a significant fraction of the clock period. The waveform often resembles a sinusoidal wave, so the metastability is unavoidable.

This paper presents a detailed analysis of the metastable behavior in the CML latches. Section-2 briefly describes the operation of the CML latch. In Section-3 metastability dependence on the rise/fall time of the clock signal is derived. Section-4 presents 0.18 \textmu m CMOS technology simulation results to verify the correctness of the presented analysis.

2. CML Latches

A conventional current mode logic latch consists of a sample and a hold stage, as shown in the Fig. 2 [2]. The current switching between the pairs takes place by the complementary signals of the clock. The sampling pair works as a CML buffer and when it is activated by the clock signal, it keeps track of the input data and transforms it to the outputs. This is known as the sampling mode of the latch. When the clock polarity changes the hold pair becomes active. The cross-coupled transistors in the hold pair form a regenerative positive
feedback structure and keep the output data at the current state. This is known as the hold mode because the output is isolated from any changes in the input data, as no current is flowing through the sampling pair.

A properly biased CML circuit has all the biasing current $I_S$ flowing through either one of the two branches. Due to a voltage drop across the load $R_L$ the low output voltage becomes $V_L = V_{DD} - I_S R_L$. The other output of the branch with no current remains at the high voltage $V_H = V_{DD}$. The output voltage swing $\Delta V$ is therefore $V_H - V_L = I_S R_L$. Ideally all the input and output signals have the same voltage swing with a common mode voltage $V_{CM} = V_{DD} - \Delta V/2$.

Let $I_1$ and $I_2$ be the currents flowing through the two loads, and $I_{sample}$ and $I_{hold}$ be the currents flowing through the sample and the hold pairs respectively. The total capacitance at the output of the latch is given by

$$C_O = C_L + C_j + C_{Hold}$$

where $C_L$ is the load capacitance, $C_j$ is the drain to bulk junction capacitance and $C_{Hold}$ is the parasitic capacitance of the cross-coupled hold pair. It is interesting to note that both outputs see different output capacitances during the sample and the hold mode, because of the change in the operating region of active devices [3]. Let $C_{j+}$, $C_{j-}$, $C_{H+}$ and $C_{H-}$ be the output capacitances of the positive and negative outputs during the sample and hold modes respectively. Table 1 summarizes the total capacitance at the output terminals in both modes of latch operation. These unequal output capacitances result in unequal rise and fall times. It is assumed that the CML latch is driving the same size CML latch or buffer. The load capacitance $C_L$ will also vary depending on the biasing conditions of the following stage.

![Fig. 2. A conventional CML latch.](image)

### 3. CML Latch Delay Analysis

Any change in a signal with a finite slew rate will take some time for the input charging to threshold and internal device turning on, denoted by $T_i$, which depends on the size and biasing conditions of the device. After this delay the current flowing through the device changes immediately and charging or discharging of output capacitance starts. $T_i$ delay is usually small as compared to the output charging time. Different transition time for the data and the clock will have different impact on the latch propagation delay. For the following analysis it is assumed that the rise/fall time of the data and clock signals are the same and denoted by $T_r$.

![Fig. 3. Signal waveforms to illustrate the terminologies used.](image)

#### 3.1. Delay in the Stable Region

If the last change in the data is during the transparent mode of the latch well before the triggering edge of the clock, the output will change accordingly after a certain delay $T_{DQ(Stable)}$. If the data changes from a low input voltage $V_L$ to a high input voltage $V_H$ in time $T_i$, consequently after $T_r$ delay the flow of current will switch in the branches from $I_1$ to $I_2$ in time $T_r$. Still all the current is flowing through the sample pair, because...
there is no change in the clock signal. Once the current transition starts, the output starts charging and during the current transition it will be charged up to a final value \( V_O \)

\[
V_O = V_L + \frac{1}{C_S} \int_0^{T/2} I_i \, dt = V_L + \frac{1}{C_S} \frac{I_s T_r}{2} \tag{2}
\]

At this point the current reaches a stable value of \( I_S \) and the charging process continues. Time required to charge the output to the mid-swing voltage level \( V_M \) is given by

\[
T = \left( V_M - V_L \right) - \frac{1}{C_S} \frac{I_s T_r}{2} + \frac{1}{C_S} \Delta V - \frac{1}{2} T_r \tag{3}
\]

so the propagation delay in the stable region is given by

\[
T_{DQ(S)(Stable)} = T_i + \frac{1}{2} T_r + \frac{1}{2} \frac{C^+}{I_S} \Delta V - \frac{1}{2} T_r = T_i + \frac{1}{2} \frac{C^+}{I_S} \Delta V \tag{4}
\]

Note that the delay is taken as the time from 50% input to the 50% output charging.

3.2. Limit of the Stable Region

Limit of the stable region is \( T_{DQ(Stable)} \) (see Fig.1), for which there is no increase in the latch delay from its stable value \( T_{DQ(Stable)} \). It is only possible if the outputs are already charged to \( V_M \), just before the current starts to flow from the sample to the hold pair. Current transition starts \( (\sqrt{2} T_r - T_i) \) time earlier than the clock edge.

\[
T_{DQ(Stable)} \geq T_{DQ(Stable)} + \frac{1}{2} T_r - T_i = \frac{1}{2} \frac{C^+}{I_S} \Delta V + \frac{1}{2} T_r \tag{5}
\]

Although the total bias current will split between \( I_{sample} \) and \( I_{hold} \) still all the current will be flowing through the same branch \((I_1 \text{ or } I_2)\). But there will be some change in the output rise time due to the decrease in the output capacitance, \( C_H \), as the hold pair is now in active region. It is clear from (5) that the setup time increases with \( T_r \).

3.3. Delay in the Metastable Region

If the data changes after \( T_{DQ(Stable)} \), the output will not be charged to \( V_M \) before the current switching starts. \( I_{sample} \) will decrease gradually and \( I_{hold} \) will increase at the same time. The hold pair will try to regenerate the data, opposing the sampling pair. During the first half of current transition \((T_r /2)\), the current flowing through the sampling pair is larger than the current flowing through the hold pair. Therefore,

\[
Output \, \text{Charging} = \text{Charging (Sample)} - \text{Discharging (Hold)} \tag{6}
\]

Depending on the level to which the output was previously charged, it is possible that the output will be charged up to \( V_M \) during the time \( T_r /2 \). The hold pair would then regenerate it correctly. This would result in a longer delay and a longer rise time. This is known as the metastable region where the latch’s delay \( T_{DQ} \) increases exponentially with smaller \( T_{DC} \).

3.4. Limit of the Metastable/Failure Region

If the output fails to charge to \( V_M \) during the first half of current transition the hold pair regenerates to a wrong value and the latch operation fails. The metastable region is limited by \( T_{DC(min)} \) for which the output is charged to \( V_M \) just before the current through the hold pair exceeds from that of the sample pair. Using (6), the output charging to \( V_M \) during the half current transition is

\[
\frac{3}{8} \frac{I_s T_r}{C^+} - \frac{1}{8} \frac{I_s T_r}{C^+} = \frac{1}{4} \frac{C^+}{I_s} \tag{7}
\]

and the initial charging during the data transition, from (2), is

\[
V_O = V_L + \frac{1}{2} \frac{I_s T_r}{C^+} \tag{8}
\]

so the time used for charging with stable current \( I_S \), is

\[
T = \left( V_M - V_L \right) - \frac{1}{2} \frac{I_s T_r}{C^+} + \frac{1}{2} \frac{I_s T_r}{C^+} \frac{C^+}{I_s} \Delta V - \frac{3}{4} T_r + \frac{1}{2} T_r
\]

now the total time taken for output charging to \( V_M \) is given by

\[
T_{DQ(max)} = T_i + \frac{1}{2} T_r + \frac{3}{4} \frac{C^+}{I_S} \Delta V + \frac{1}{2} T_r \tag{9}
\]

since the current switching takes place \( T_i \) delay after the clock edge, the corresponding \( T_{DC(max)} \) can be obtained as follows

\[
T_{DC(min)} = T_{DQ(max)} - T_i = \frac{3}{4} \frac{C^+}{I_S} \Delta V + \frac{1}{4} T_r \tag{10}
\]

Any change in the data after this time will not be captured by the latch. And the hold pair will regenerate the output to its previous value. An unwanted bump at the output will appear, as shown in Fig. 4. Equations (5) and (9) define the boundaries of the metastable region, which is clearly dependent on \( T_r \).

4. Simulation Verification

The presented analysis is based on an assumption that the biasing current \( I_S \) remains constant during the switching of data
and clock signals. However, in reality, as it could easily be observed in simulation, the current $I_S$ varies during switching. The first effect is that during the current commutation between the sampling and holding branches the instantaneous conductance of both branches can be low, causing the total current to drop. This can be prevented by careful selection of DC biasing of clock and data signals. The second effect is caused by the $C_{DS}$ parasitic capacitance of the current sourcing transistor. This effect is difficult to avoid especially in a low-voltage design where the $V_{DS}$ voltage drop is minimized by increasing the $W/L$ ratio of current biasing transistor. Interestingly, the resulting current peaking effect may improve the performance of the latch circuit. The results of this investigation will be reported in a separate publication.

Fig. 5. Simulation test bench.

A test bench is set-up as shown in Fig. 5 to simulate the effect of $T_r$ on the latch timing parameters. TSMC 0.18µm CMOS technology was used as an example. Series input resistors $R_{in}$ are used to realize the input charging time $T_i$, using ideal sources. $T_{DC}$ is swept from the stable region to the failure region and the corresponding latch delay $T_{DQ}$ is plotted. Fig. 6 shows the simulation results, with different values of $T_r$. It can be observed that during the stable region the delay does not depend on $T_r$, as predicted by (4). The setup time and the width of metastable region are also proportional to the rise/fall time. The latch delay before failure $T_{DC(max)}$ is found to be much higher in simulation than what was predicted in (8). This is due to the drop in total bias current $I_S$, as explained earlier in this section.

Fig. 6. CML latch delay with different rise/fall times.

5. Conclusion

This paper addressed the issue of metastable behavior in CML latches. A detailed analysis was presented to show the dependence of characteristic latch parameters on the rise/fall time of the clock signal. In fact the latch/flip-flop timing parameters are the issue of reliability of the system. This analysis would allow the designers to find the optimum setup time for the latches/flip-flops, in order to use every fraction of the clock period. The optimum setup time lies within the metastable region [4], whose boundaries are determined by the current switching time. Hence the rise and fall times of the clock signal strongly affect the performance of a latch or flip-flop. Based on this analysis, the circuit re-optimization will result in increased speed and reliability of the system.

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