AN ALL-DIGITAL DATA RECOVERY CIRCUIT OPTIMIZATION USING MATLAB/SIMULINK

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ABSTRACT
The design of an all-digital Data Recovery (DR) circuit requires careful system-level design space exploration. The advantages of an all-digital implementation are the ease of portability and reduced time-to-market across fabrication processes and with reducing feature sizes. For a selected architecture, this paper explores the effects of sweeping the bit detection interval of a bang-bang phase detector, the phase update interval, and the number of clock phases used for data recovery using a Matlab/Simulink model. The simulation results show the variation of jitter tolerance of the DR circuit with respect to the above parameters. An all-digital architecture can be made adaptive to jitter conditions, if the design trade-offs are known a priori. A statistical graphing/analysis tool is used to present the 3D logarithmic scatter plots.

1. INTRODUCTION
Conventional Clock and Data Recovery (CDR) circuits perform a 2x oversampling of the data. More specifically, one of the edges is aligned using a timing recovery Phase-Locked Loop (PLL) and the other edge is used to sample the data. In case of a clock with a 50% duty cycle, this sampling edge would be 0.5 Unit Intervals (UI) later. In the presence of excessive total asymmetric jitter, the sampling point may not be ideally located at the centre of the eye thereby causing a bit error if conventional 2x oversampling is used. An all-digital eye-tracking 3x oversampling method has been presented [1] to provide enhanced high-frequency jitter tolerance at 2.5 Gb/s whereas a jitter-boundary tracking, variable interval 3x oversampling method proposed in [2] achieves similar results at 5 Gb/s, although the implementation is mixed-signal. Another category of oversampling CDR circuits is the phase-picking architecture [3] or the blind-oversampling architecture [4]. In this scheme, the incoming bits are oversampled by an odd multiple and are accumulated in a First-In-First-Out (FIFO) buffer so that edge detection can be performed. Jitter statistics are gathered in real time. The data is then recovered by either implementing a majority voting algorithm or by picking the sample farthest from the bit boundary. A PLL is not apparent in such implementations but is present algorithmically, nevertheless.

A review of modern phase detectors is presented in [5]. It can be seen that the Bang-Bang Phase Detectors (BBPD) find increasing use in the modern CDR circuits since they provide several circuit-level benefits namely; no limiting preamplifiers, no charge-pumps, no sampling uncertainty, possibility of sampling multiple bits in the same clock period resulting in a lower frequency clock with reduced jitter, and suppression of pattern-dependent jitter for tri-state implementations. Analysis of jitter caused by a BBPD in a PLL-type CDR is an area of active investigation [6].

Two popular architectural choices for the BBPD are: using the multiple phases of the clock [5] as shown in Figure 1(a) or employing the delayed versions of the data itself [1] as shown in Figure 1(b). Multiple phases of the clock generally require a locked oscillator and increase the power dissipation and complexity of the circuit, whereas multiple delayed versions of the data allow for a simpler and power-efficient design. A relative advantage of a multiple clock phase architecture is that a VCO can be locked to the frequency of the incoming data to implement a rate-agile CDR. Also, the delays remain well controlled due to the locked oscillator.

![Figure 1. BBPD architectures](image)

2. ARCHITECTURE OVERVIEW
The architecture used for this design-space exploration is based on [1] with some modifications based on our requirements. The block diagram of the architecture is shown in Figure 2. In order to make use of the theory already presented in [1], a few terms are redefined here for the sake of convenience.

- **D_IN**: Serial data input to the DR circuit
- **R_DATA**: Recovered Data
- **R_CK**: Recovered Clock (Selected Phase)
- **UP/DN**: Outputs of the BBPD
- **INC/DEC**: Outputs of the Digital Filter

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Clock phase selection signals

Number of clock phases

Clock dividers that divide $R_{CK}$ by $L$ and $M$ respectively to clock the Digital Filter and the Phase Selection Unit ($L = 2$)

As described in Figure 1, the delay value through the BBPD delay blocks

The data ($D_{IN}$) comes into the BBPD and three delayed versions are created. The UP and DN signals are generated by the BBPD and the Digital Filter decides to either slow down (INC) or speed up (DEC) the clock phase every $M$ bits. For the purpose of behavioral Simulink exploration that follows, an ideal clock generator with $N$ phases is being used at the data frequency. The phases are selected such that if the phase is advanced beyond phase-‘$N−1$’, it simply rolls over to phase-‘0’ thus providing an unlimited phase range for the DR circuit as proposed in [1]. A similar mechanism works in the other direction. The clock generator could be a locked voltage-controlled oscillator (VCO) or an independent Delay-Locked Loop (DLL) with some associated feedback control circuitry as required by the application.

Figure 2. Block Diagram of the architecture

3. SIMULATION SETUP

Our objective is to setup a simulation (Figure 3) where serial data (2.5 Gb/s Non-Return to Zero (NRZ)) with added sinusoidal jitter is recovered. For the jitter tolerance trends, the bit detection interval of the BBPD ($T_{del}$), the phase update period ($M$ bits), and the number of clock phases ($N$) are swept. The modulated clock is generated by using a Sine Wave block driving a Phase Modulator block from the Simulink libraries. It drives a Linear Feedback Shift Register (LFSR7) that introduces a $2^7$-1 Pseudo-Random Bit Sequence (PRBS) into the DR circuit under test. The recovered data is phase-compared with the original data and an integrate-and-dump circuit detects the residual phase error per bit.

A typical 2 µs simulation is shown in Figure 4 (5000 bits are not shown) where the DR circuit comfortably tracks a 0.5 MHz sinusoidal jitter with an amplitude of 8.6 UI peak-to-peak. Other parameters are, $M = 16$, $T_{del} = 0.25$ UI, and $N = 8$. The important

Figure 4. Typical simulation Result (a) Selected Phase Number (b) Amplitude of added sinusoidal jitter (c) Residual Phase error

points annotated to the simulation are described below.

A Phase of the jitter sinusoid starts (arbitrarily) at $\pi/2$ so that the DR circuit locks faster and simulation time can be saved.

B Phase decelerating to catch up with jitter (INC)

C Flat portion where no tracking happens for a period corresponding to $T_{del}$. Also see the corresponding ‘F’ and ‘H’ annotations.

D Phase accelerating to catch up with jitter (DEC)

E Points of maximum slope on the jitter sinusoid

F Flat portion of jitter sinusoid

G Residual error when tracking occurs

H Error accumulates when there is no tracking

I Error holds steady with a level-shift. A spike reaching a $+1$ threshold signals an incorrect bit.
It is clear that if the absolute slope of the tracking waveform is less than the slope of the jitter sinusoid at points ‘E’ in Figure 4, then the tracking would not be possible. The slope of the tracking waveform is determined by the magnitude of the phase jump \( (UI/N) \) and the minimum update period of \( M \) bits. The Digital Filter also affects the decision based on the amount of jitter present. The value of \( T_{del} \) determines if a bit boundary is detected by the currently selected clock edge in the BBPD. A high value would cause more activity in the Digital Filter and deteriorate the high-frequency jitter tolerance. A low value would imply a diminished wander tracking capability. The jitter tolerance is therefore a function of the three main parameters of the digital PLL as described in [1]

\[
\text{Jitter Tolerance} = f(T_{del}, M, N),
\]

where the symbols have their pre-defined meanings.

4. SIMULATION RESULTS

A base parameter set is chosen \((T_{del} = 0.25 \text{ UI}, M = 16 \text{ bits} & N = 8 \text{ phases})\) and the selected parameter is swept. The final optimization will maintain the presented trends and has to be done recursively.

4.1 Jitter Tolerance vs. \( T_{del} \)

![Figure 5. Jitter Tolerance vs. \( T_{del} \)](image)

Figure 5 shows the parametric jitter tolerance curves on a logarithmic 3D-scatter plot [8] while sweeping the \( T_{del} \) parameter from 0.10 UI to 0.40 UI. It is difficult to see the trend from Figure 5 so an averaging operation was performed and a surface plot was created as shown in Figure 6. The x-axis is not logarithmic as the tool doesn’t allow it, but we are interested in the y-axis view that shows the variation of \( T_{del} \). It can be seen that the high-frequency jitter tolerance has a negative slope with a significant variation near \( T_{del} = 0.15 \text{ UI} \), whereas the low-frequency tracking has a positive slope. Hence a choice of \( T_{del} = 0.25 \text{ UI} \) seems appropriate since there are no major variations in the high-frequency jitter tolerance around this point. Also, the DR circuit bandwidth does not change significantly beyond \( T_{del} = 0.20 \text{ UI} \) as can be seen in Figure 6 by noticing its wander tracking capability. Given this finding, if multiple phases of a locked VCO are used to sample the data in the BBPD, then the percentage variation is limited by VCO phase noise and jitter, which is typically very low. If the \( T_{del} \) blocks are implemented using simple CMOS elements, a deviation of 10% in the value of \( T_{del} \) due to Process-Voltage-Temperature (PVT) variations can cause a 30% change in the tracking ability. This may result in frequent loss-of-lock under heavy jitter environments. With a changing bandwidth, re-acquiring lock would require additional circuitry. Analog stabilization techniques for temperature, bias and delay could be used but the all-digital advantage would be lost. After the Simulink-based parameter optimization, a circuit simulator can study this effect as part of the chip design-flow.

4.2 Jitter Tolerance vs. Phase Update Period (\( M \))

The DR circuit bandwidth is inversely proportional to the update period \((M)\). The update period also affects total power, since the phase selection unit is logic-intensive. Figure 7 shows that the tracking capability and the bandwidth of the DR circuit display an inversely proportional log\(_{2}\) dependence with increasing \( M \). The y-axis has a log\(_{2}\) scale whereas the x- and z- axes have a log\(_{10}\) scale. The curves are shown mirrored for increased bandwidth visibility. The \( M \) divider can thus be used to provide more tunability.

![Figure 7. Jitter Tolerance vs. Update Period \( M \)](image)
4.3 Jitter Tolerance vs. Clock Phases \((N)\)

Figure 8 shows the variation of jitter tolerance with the number of clock phases \((N)\). If the number of phases is high, then the DR circuit can only compensate for smaller amounts of jitter accumulated during the same phase update period. The low-frequency wander tracking capability suffers with an increasing number of clock phases but jitter transfer performance improves with increasing \(N\).

![Figure 8. Jitter Tolerance vs. clock phases \((N)\)](image)

4.4 Relative dominance of parameters

Table 1/Table 2 show the relative dominance of the three parameters discussed in this paper for low-frequency wander tracking capability and the high-frequency jitter tolerance respectively. It can be seen that bit-detection interval \(T_{\text{del}}\) has a conflicting influence on low and high-frequency jitter tolerance results, whereas \(M\) and \(N\) mainly affect the low-frequency wander tracking capability.

5. CONCLUSIONS

- The exploration of the design-space for the Data Recovery circuit based on [1] was performed using Matlab/Simulink. It can be seen that an all-digital Data Recovery circuit with a high good-high frequency jitter tolerance (0.7 UI p-p) can be implemented without requiring a synchronized VCO circuit.
- The BBPD architecture plays a dominant role in the high-frequency as well as the low-frequency jitter tolerance behaviors. The delayed versions of the data provide a power and area-efficient realization of the BBPD in the digital DR circuit.
- Three parameters were swept to establish their relative influence on jitter tolerance. These were the delay value for edge-comparison in the BBPD \((T_{\text{del}})\), the phase update period \((M)\) and the number of clock phases \((N)\). The \(T_{\text{del}}\) parameter has a strong conflicting influence on the low-frequency wander tracking capability and the high-frequency jitter tolerance of this DR circuit.

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7. REFERENCES