NEW CML LATCH STRUCTURE FOR HIGH SPEED PRESCALER DESIGN

Muhammad Usama and Tad Kwasniewski
Department of Electronics, Carleton University,
1125 Colonel By Drive, Ottawa, Ontario, K1S 5B6 Canada.
{musama, tak}@doe.carleton.ca

Abstract

This paper emphasizes on the design and analysis of Current Mode Logic latches and their application in a frequency prescaler. Operation of a conventional CML latch is analyzed and a clock feedback structure is proposed for increased stability with reduced delay parameters. A low power design technique is presented for Current Mode Logic frequency prescalers, which allows the Master and Slave latches to be merged together so that they use a single current source. This significantly reduces the power consumption and area and also offers lower terminal capacitances resulting in faster circuit operation.

Keywords: Current Mode Logic (CML); Clock Feedback Latch; Frequency Prescaler.

1. INTRODUCTION

A frequency prescaler is the key component in a PLL synthesizer for the translation from high to low frequencies. Digital frequency dividers are the most popular divider structures in use today. They offer flexible programmability, higher division ratios and easier digital control. The fundamental element of a digital frequency divider is a flip-flop, or two level-sensitive latches in master-slave configuration. A wide variety of D-flip-flop circuits have been reported in the literature. Recently interest in Current Mode Logic has increased due to its superior performance at very high frequencies as compared to other logic styles. CML latch was first introduced in [4] and some modified latches are found in literature [2][3]. The CML latches exhibit better performance than other latch structures.

Prescalers are one of the critical parts of the system because they operate at the highest frequency. This is the key point for the high-speed operation and low power consumption [3]. A clock feedback latch structure can be used to minimize the latch delay and setup time. The master and slave latches can be combined together to reduce the power consumption at the same operating frequency.

This paper presents the design and analysis of CML latches and prescaler. Section-2 briefly describes the operation of general CML circuits. It also covers the review of a conventional CML latch. A modified latch design is presented in Section 3. A low power technique for high frequency CML prescaler is presented in Section 4. Simulation results are presented in Section 5.

Fig. 1: General CML Structure

2. CURRENT MODE LOGIC

2.1 CML Circuits

In general CML circuits consist of three main components, as shown in Fig. 1, which include the pull-up load, the pull-down network (PDN) and a constant current source [4]. CML is a completely differential and static logic. Due to its differential nature, it is highly immune to common mode noise. Depending on the input combination and the logic implemented by the
PDN, all the current flows through one of the two branches, providing complementary output signals. Voltage at the output of branch with no current reaches $V_{DD}$, whereas for the other branch some voltage drops across the load resistor and the output voltage becomes $V_{DD} - I_{bias}R_L$. CML does not provide a rail-to-rail output swing, reduced voltage swing makes it faster due to quick voltage transition. It has almost flat power curve over a wide range of frequency as opposed to other logic styles where power consumption increases directly with frequency. Therefore at very high frequencies its power consumption is comparable or lower than other logic styles. This makes it a good choice for high speed and low power integrated circuit design.

![Fig. 2: Conventional CML Latch](image)

### 2.2 Conventional CML Latch

A conventional current mode logic latch consists of a sample and a hold stage. As shown in the Fig. 2 the current switching between the pairs takes place by the complementary signals of the clock. The sample pair works as a CML buffer and when it is activated by the clock signal, it keeps track of the input data and transforms it to the outputs. This is known as the sampling mode of the latch. When the clock polarity changes the hold pair becomes active. The cross-coupled transistors in hold pair form a regenerative positive feedback structure and keep the output data in the same previous state. This is known as the hold mode because the output is isolated from any changes in the input data, as no current should be flowing through the sampling pair. In the stable region the propagation delay ($D-Q$) is a function of the total output capacitance and load resistance, $T_{DQ} = C_{TOT} R_L$. If the data changes near the clock edge the $D-Q$ delay increases due to finite current transition time and causes metastability in the output.

![Fig. 3: Clock Feedback Latch](image)

### 3. CLOCK FEEDBACK LATCH

Desirable characteristics of any latch include small propagation delay in the sampling mode and isolation from the data in hold mode through current switching, but due to the device overlap capacitance, the input output coupling and clock feed through can also be observed. Using the capacitive feedback can eliminate this problem [2]. However any additional capacitance connected at the output should be avoided because it will result in higher $D-Q$ delay. Cross-coupled capacitors connected at the Clk transistors will neutralize the effect of clock feed through. At high frequencies these capacitors can result in spikes at the output due to sharp clock edges. The addition of a series resistance can suppress these spikes. However a purely resistive component will try to equalize the differential outputs resulting in failure of the latch operation. So a high resistance is required for clock feed through cancellation. A cross-coupled feedback transistor pair at the Clk terminals will suffice the requirement of both the capacitor and resistor, as shown in Fig. 3. This does not improve the performance in the stable region as can be seen in Fig. 8 that the Clk-Q delays are same. But it significantly reduces the minimum setup time before the failure region. It also results in reduced dynamic power dissipation due to stable output. Simulation results are presented in Table-I.

The aspect ratio of feedback transistors $(W/L)_{FB}$ should be kept small for higher resistance, whereas larger width is required for more capacitance. However larger $(W/L)_{FB}$ will create instability and spikes at the output, or complete failure at the extreme. So careful sizing must be performed according to other transistor sizes and currents in the latch.
4. PRESCALER DESIGN

A CML prescaler combines two level-sensitive CML latches in master-slave configuration, as shown below in Fig. 4. Depending on the division ratio a number of master slave latches can be cascaded, and the inverted outputs of the last stage are fed back to the first stage.

![Conventional Master-Slave Latches](image)

In a conventional CML latch the transistor sizes of the sample and the hold pair must be the same because the same current passes through one of the two transistor pairs due to the complete current switching depending on the clock signal. Because of the parasitic capacitance of transistors of sample circuit, the tail current must be sufficiently high to achieve a higher slew rate and a larger transconductance. On the other hand the hold circuit do not need a large bias current. In reference [2], the regenerative latch is modified so that the sample circuit and the hold circuit use two distinct tail currents. This technique shows significant improvement. However this increases the static power consumption and circuit complexity.

The master and slave latches can be combined as shown in Fig. 5 so that they use a common current source and are switched by the same pair of clock transistors.

![Master-Slave Latches Combined](image)

Smaller transistor sizes for the hold pairs of latches can be used to make most of the current flow through the sample pair and eliminates the need of using two distinct current sources. Due to the lower current through hold pair the current source does not need to be double, but a 1.5 times transistor width is sufficient for the successful operation at the same operating frequency. This reduces the static power dissipation. This technique is also area efficient, because the current source is the dominant area-occupying component. Using single current source and clock transistors save up to 20% of the layout area. Small transistor sizes offer lower diffusion capacitance at the output terminals, which results in lower D-Q delay and higher operating frequency.

![Fig. 5: Master-Slave Latches Combined](image)

![Fig. 6: Illustration of minimum clock period](image)

Maximum operating frequency of a divider is bounded by the sum of Clk-Q delay and the setup time. If the output changes after the setup time, near the clock edge, it will cause metastability resulting in higher division ratio. Clock feedback transistors can minimize the setup time as can be seen in Fig. 8. This reduces the minimum required clock period and allows the signal division at higher input frequencies. Fig. 7 shows a schematic of a divide by 2 prescaler with master slave latches combined and clock feedback transistors in place.

![Fig. 7: Schematic of a Divide by 2 Prescaler](image)
5. SIMULATION RESULTS

Simulations were performed in a 0.18μm CMOS technology. The minimum D-Q delay is the only true measure of the performance of a master-slave latch or flip-flop [1]. Fig. 8 shows the curves of D-Q and Clk-Q delays versus D-Clk delay. It can be seen that the feedback latch has smaller minimum D-Q delay than the conventional latch.

![Fig. 8: Delays of Conventional and Clock Feedback latches](image)

The clock feedback latch also exhibits lower setup and hold times. Simulation results are summarized in Table-I. Although the internal power dissipation is a bit higher, it is compensated by the higher operating frequency resulting in lower power delay product. Table-II shows the comparison results of a master-slave combined prescaler, normalized with the conventional prescaler. The combined prescaler has lower power dissipation, smaller die area, higher maximum operating frequency and wider operation bandwidth that can be seen in Fig. 9.

![Fig. 9: Operating frequency range of Conventional and Combined divide by 2 Prescalers](image)

### Table-I: Comparison Results of Conventional and Proposed Latches

<table>
<thead>
<tr>
<th>Simulation Parameter</th>
<th>Conventional Latch</th>
<th>Proposed Latch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Dissipation (μW)</td>
<td>&lt;265</td>
<td>&lt;275</td>
</tr>
<tr>
<td>Power Delay Product (f J)</td>
<td>&lt;45</td>
<td>&lt;30</td>
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</table>

### Table-II: Comparison of Conventional and Combined Prescaler (Normalized)

<table>
<thead>
<tr>
<th>Type (Normalized)</th>
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<th>Master-Slave Combined</th>
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<td>Power Dissipation</td>
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<tr>
<td>Layout Area</td>
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<td>Maximum Frequency</td>
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<tr>
<td>Operation Bandwidth</td>
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<td>1.4</td>
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6. CONCLUSIONS

In this paper a modified CML latch structure with feedback clock transistors is presented which increases the stability and performance measures. A technique for low power prescaler design is proposed which combines the master and slave latches with a common current source and the same clock transistors. This technique effectively reduces the power consumption and chip area. The Master-Slave combined latch with clock feedback transistors is a good choice for high speed and low power CML Prescalers.

References


