A VLSI Implementation of an Adaptation Algorithm for a Pre-Emphasis in a Backplane Transceiver

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Abstract—Two different hardware structures of a sign-sign block least-mean-square (LMS) algorithm for an adaptive pre-emphasis in a backplane transceiver have been implemented in Verilog targeting the TSMC 0.18mm CMOS technology. Functional models and Matlab code have been developed to simulate a transceiver system for both structures. A pulse amplitude modulated four-level (4-PAM) signaling technique is used in the Matlab simulation. Results show that the proposed parallel adaptation engine is four times faster than the published round-robin adaptation engine in terms of coefficient update rate with comparable hardware. Both circuits prove that digital CMOS18 standard cells can be used directly to achieve 625 MHz timing constraints. A custom circuit is not needed to implement the digital adaptation algorithm for the analog adaptive pre-emphasis up to 625 MHz.

Keywords: LMS, 4-PAM, pre-emphasis, backplane transceiver

I. INTRODUCTION

The ever-increasing need for high data rate in communication systems is driving data transmission within networking equipment to multi-gigabit per second rates. Copper backplane based serial transmission is one of the most commonly used techniques in high-speed transmission due to its lower cost, reduced complexity and high reliability.

Although a copper backplane offers significant advantages in high-speed transmission, it does have some technical challenges, mainly because of distortion due to skin effect, dielectric loss and reflections. This results in “eye-closure”, and therefore, high Bit Error Rate (BER) at the receive end.

In order to reduce BER, compensation for the channel transfer function is often used. In general, there are three possible equalization techniques used to reduce distortion caused by the channel. These are transmit pre-emphasis, receive equalization or a combination of the two.

Pre-emphasis offers significant advantages, such as, lower power consumption, superior performance and better interoperability. Pre-emphasis can be divided into three categories, i.e., fixed, programmable, and adaptive pre-emphasis. The first two need expensive test equipment during development and are not suitable for a wide variety of backplane lengths, materials, and connectors. Also, robust operation at data rates of up to 5 Gb/s requires tracking and compensation for changes in environmental conditions, such as power supply, temperature, and aging [1].

This paper presents a novel VLSI implementation of an adaptation algorithm for an adaptive pre-emphasis scheme. Section II presents the Matlab simulation models, adaptation algorithm, and some simulated results. Section III details hardware implementations of two structures. Conclusions are presented in Section IV.

II. FUNCTIONAL SIMULATION

A. Matlab Simulation Model

A Matlab simulation model provides proof of concept and facilitates the functional verification of the backplane transceiver with the published and proposed adaptation engines before they are implemented in hardware. The simulation model is shown in Fig. 1. The complete Matlab simulation code for adaptive pre-emphasis is developed.
This simulation model includes the following sub-models: 4-PAM Generator, Pre-Emphasis, Digital-to-Analog Converter (DAC), Channel Model, AWGN Generator, and Adaptation Engine.

The 4-PAM Generator creates random 4-PAM data as input using the rand and ceil functions.

The Pre-Emphasis is modeled as an adaptive FIR filter with four taps, as shown in Fig. 2. $s_r$ is the main data sample. $w_L$, $w_M$, $w_T$, and $w_R$ are continuous coefficients for the leading, main, trailing and rover taps respectively. The leading tap ($w_L$) and trailing tap ($w_T$) are used to cancel ISI caused by the precursor and postcursor. The main tap ($w_M$) adjusts the amplitude of the transmitted signal to ensure that the received signal is within a desired range. The rover tap ($w_R$) is used to cancel reflections due to discontinuities and imperfect terminations of the transmission lines.

The DAC converts digital tap coefficients to analog tap values for the pre-emphasis. Resolutions for the leading tap, main tap, trailing tap, and rover tap are 5-bit, 6-bit, 6-bit and 4-bit, respectively. The AWGN Generator is implemented to emulate white Gaussian noise. The Adaptation Engine implements the sign-sign block LMS adaptation algorithm and passes the updated coefficients to the input of the DACs. Channel Model is a 30-inch FR4 circuit model from Altera Corporation. The channel loss for this channel model is shown in Fig. 3.

B. Adaptation Algorithm

The least-mean-square (LMS) algorithm is the most popular algorithm for the implementation of adaptive filters. In order to simplify hardware implementation, some variants of the LMS algorithm were proposed, such as sign-data LMS, sign-error LMS, and sign-sign LMS [2]. This research uses the sign-sign block LMS algorithm [1] for the adaptation process. The adaptation equations for the digital representation of the taps for block $j$ are given by equation (1).

$$
\begin{align*}
c_L(j+1) &= c_L(j) + \alpha \sum_{i=0}^{L-1} \text{sign}(e_i) \text{sign}(d_{i+1}) \\
c_M(j+1) &= c_M(j) + \alpha \sum_{i=0}^{L-1} \text{sign}(e_i) \text{sign}(d_i) \\
c_T(j+1) &= c_T(j) + \alpha \sum_{i=0}^{L-1} \text{sign}(e_i) \text{sign}(d_{i-1}) \\
c_R(j+1) &= c_R(j) + \alpha \sum_{i=0}^{L-1} \text{sign}(e_i) \text{sign}(d_{i-M})
\end{align*}
$$

Where $C_L$, $C_M$, $C_T$, and $C_R$ are digital coefficients for the leading, main, trailing, and rover taps. $L$ is the length of the input data block. The subscripts on the error ($e$) and data ($d$) indicate their position within the data block. The
function \( \text{sign}(x) \) is +1 when its argument is greater than or equal to 0 and \(-1\), otherwise.

C. Simulation Results
The performance of the adaptive pre-emphasis can be verified via passing a 200ps pulse through the channel. Fig. 4 shows an example of a pulse response with and without pre-emphasis. The sampling times are marked on the x-axis. Note that near zero ISI is achieved.

The performance of the adaptive pre-emphasis can also be verified via an eye diagram. Fig. 5 shows the channel output without and with the pre-emphasis. These figures show significant improvement in the eye opening using adaptive pre-emphasis. The simulation proved that the sign-sign block LMS algorithm is a simple and efficient adaptation algorithm, which effectively compensates for ISI caused by copper backplane channels. For the simulation, the bias current settings are extremely important for the DAC with limited resolutions and must be selected very carefully. A data block size of 1024 was used for the hardware simulation.

III. HARDWARE IMPLEMENTATION
Two different hardware structures for the adaptation algorithm circuit were implemented in Verilog targeting the TSMC 0.18\(\mu\)m CMOS technology. Both circuits show that standard cells in the CMOSPIB technology can be used to achieve the necessary 625 MHz timing constraints.

A. Digital Round Robin Adaptation Engine
The first adaptation algorithm circuit structure is the round robin adaptation engine, as shown in Fig. 6 [1]. The 8-bit shift register and the associated 4:1 multiplexer are used to select the correct “sign of the data” for each tap. A single flip-flop is used to provide a delayed version of the “sign of error”, which is required in equation (1). The multiplication of the sign of data and the sign of error is realized by using an XOR gate. Consecutive XOR outputs are accumulated in an up/down counter and the sign of the result is captured in a latch bank. The sequencer is the controller of the adaptation engine. It consists of a counter that generates a summation period control signal that is sent to the up/down counter. This control unit also changes the tap position after each block of data. When all tap adjustments have been determined, a control signal generated by the sequencer is sent to the message generator.
to create the digital tap coefficients that are fed back to the coefficient DACs in the transmitter.

Fig. 6 Digital round robin adaptation engine

B. Digital Parallel Adaptation Engine

In order to speed up coefficient update rate and to relax the critical path delay from the output of the 8-bit shift register to the input of the up/down counter, a parallel adaptation engine is proposed, as shown in Fig. 7. In this structure, all tap coefficients are updated at the end of each block of data. All blocks in Fig. 7 have the same functionality as in the round robin adaptation engine except that the sequencer block is much simpler. A single sequencer provides simultaneous control for all four up/down counters. At the end of each block of data, a summation control signal is sent to all up/down counters to trigger all tap update adjustments and a message control signal is sent to the message generator to create the digital tap coefficients.

Fig. 7 Digital parallel adaptation engine

C. Comparison of the Adaptation Engines

Comparison between the two adaptation engines from the synthesis results is listed in Table 1. The comparison shows that the two structures are comparable in terms of hardware requirements.

Table 1 Comparison of Synthesis Results

<table>
<thead>
<tr>
<th>Item</th>
<th>Round-Robin Adaptation Engine</th>
<th>Parallel Adaptation Engine</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-chip clock</td>
<td>500 MHz</td>
<td>500 MHz</td>
</tr>
<tr>
<td>Total Cell Area</td>
<td>113608μm²</td>
<td>122719μm²</td>
</tr>
<tr>
<td>Total Dynamic Power</td>
<td>49.3mW</td>
<td>56.8mW</td>
</tr>
<tr>
<td>Cell Leakage Power</td>
<td>1.02μW</td>
<td>1.50μW</td>
</tr>
<tr>
<td>Sequential Cells</td>
<td>111</td>
<td>126</td>
</tr>
<tr>
<td>Fault Coverage</td>
<td>99.28%</td>
<td>99.92%</td>
</tr>
</tbody>
</table>

The layouts for both adaptation engines are shown in Fig. 8. The total cell area required for logic is slightly less for the round robin but this is not an advantage as the die is pad limited. This results in the overall die size being the same for both implementations.

The parallel adaptation engine is four times faster in terms of coefficient update rate due to accumulating all tap adjustments in parallel. Also, the control block for the parallel adaptation engine is much simpler than that of the round-robin adaptation engine. It is easier to expand more taps by using the parallel adaptation engine without changing the control unit, sequencer module.

The timing constraint for both circuits was set to 2ns (500MHz) for the synthesis. The post-layout timing reports show that the worst setup slack for both circuits is 0.55ns, which means that the timing constraint for both circuits can be pushed to as high as 625MHz without timing violation. A custom circuit is not needed when implementing the digital adaptation algorithm for the analog adaptive pre-emphasis up to 625MHz.

IV. CONCLUSIONS

A detailed study of an adaptive pre-emphasis equalization scheme to improve signal quality (eye opening) for high-speed transmission (up to 5 Gb/s) on copper backplane is presented. A sign-sign block LMS algorithm is proven to be a simple and effective algorithm for the adaptation and equalization process.
Two different convergence engine structures are implemented in TSMC 0.18\textmu m digital CMOS Technology. The parallel convergence engine is four times faster in terms of convergence speed compared to the round-robin convergence engine (one block of data vs. four blocks of data) with comparable hardware requirements. Both circuits prove that digital CMOS 18 standard cells can be used directly to achieve 625 MHz timing constraints.

Also, the control block for the parallel convergence engine is much simpler than that of the round-robin convergence engine.

V. ACKNOWLEDGMENT

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REFERENCES

