The Application Of A Dual-Substrate Technique On A 10-Gb/s CMOS Phase Detector Design

Zoe Hui and Tad Kwasniewski
Electrical and Computer Engineering, Carleton University, Ottawa, Ontario, Canada
Email: zhui@ee.carleton.ca

Abstract
This paper presents a new dual-substrate technique used to overcome the small rail-to-rail supply voltage headroom available for short channel length CMOS technology. The technique is applied on a full-rate CMOS phase detector (PD) for Synchronous Optical Network (SONET) OC-192 systems. A sample-and-hold PD for 10-Gb/s Non Return Zero (NRZ) data is implemented in a standard 0.18μm CMOS technology is presented. The measurement results show that a linear range with no dead zone on phase error from -π/2 to π/2 is achieved. The core circuit dissipates a total power of 14.9 mW from a +1.6 V supply.

Introduction
As CMOS technology advances to shorter channel lengths for high speed applications, smaller rail-to-rail supply voltages make cascode configurations with more than two transistors in series difficult to implement. Low voltage circuits suffer from poor conduction in analog switches, inaccuracies in low current transistor models, lower SNR and operating frequencies [1]. In this paper, a dual-substrate technique is used to overcome the low voltage limitation problem of short channel length CMOS technologies. This technique is applied to a cascode PD design.

The challenging task in gigabit optical communication systems is the design of the Clock and Data Recovery (CDR) block in the receiver. In the CDR, the Phase Detector (PD) is a critical module and directly affects the structure and performance of the CDR. The difficulty lies on the fact that comparing the phase difference of a 10-GHz clock and a 10-Gb/s data signal is stretching the CMOS technology. In order to achieve this very high speed phase detection, PD is usually designed in GaAs or bipolar technologies, or CDR with half-rate structure or frequency divider is generally used. However, these designs struggle from high power consumption and poor jitter performance with slow settling time respectively. Therefore, a full-rate CMOS PD design will be discussed in this paper. As no paper or journal has revealed detailed design and implementation of CMOS PD at the 10-GHz range [2], the results cannot be compared with other works here. It is interesting to note that the PD developed can be used as a high speed low power master-and-slave flip-flop.

Design and Implementation

Dual-Substrate Technique

Fig. 1 shows a dual substrate technique that can be implemented in most CMOS technologies to overcome the low voltage limitation problem.

![Cross section view of silicon with dual substrate technique](image)

Here, the P-well of the NMOS transistor is reverse biased to the surrounding N-well and Deep N-well. The N-well of the PMOS transistor is reverse biased to the surrounding P-substrate. The rail-to-rail voltage is now 3.2V instead of 1.6V. The Deep N-well and P-substrate junction is not forward biased unless the P-substrate is pulled up to 0.6V. Therefore, cautious layout is required with an abundance of P+ contacts on the P-substrate to avoid its voltage from building up. One added advantage of this structure is that each transistor can be individually isolated so substrate current or noise is subsided.

Phase Detector Design

A type of PD that combines the linear characteristic of Hogge PD and the high-speed performance of non-linear Bang-Bang or Alexander PD is used. Fig. 2 shows the sample-and-hold phase detector developed [3].

Here, the activation of the master and slave states are controlled by the input data signals, Dp and Dn. The differential clock signals are sampled when the master state is turned on. When the slave state is turned on, the master state is turned off and its PMOS transistors work as resistors to prevent the holding capacitors from discharging. The slave branch samples the voltage levels stored in the holding capacitor at this time. When the
slave branch is turned off, the PMOS transistors prevent the PD outputs from discharging. The master branch is then turned on to sample the next set of clock signals. If the phase offset between the clock and data signals is constant, the PD outputs will converge to some finite DC voltage levels. State switching that creates ripples does not occur here so superior jitter performance of the loop can be achieved. PMOS transistors attached to the capacitors are operating in the triode region to eliminate the need of a common-mode feedback circuit. The circuit has a very high phase difference resolution; therefore, dead zone region is negligible and very high-speed phase detection is possible. This type of sample-and-hold PD is different from conventional sample-and-hold PD in the sense that glitch generation is not required. Differential common source drivers are used to drive the outputs, \( V_{o,p} \) and \( V_{o,n} \), to 50-ohm terminations.

**Measurement Results**

The PD was fabricated in a 0.18\( \mu \)m CMOS technology with pad-limited die area of 1.4 \( \times \) 1 mm\(^2\). Fig. 3 shows a die photograph of the PD.

**Fig. 3.** Die photograph.

A Bit Error Rate Test (BERT) system was used to test the PD. A 10-GHz signal was fed into an error performance analyzer. Differential 10-GHz clock and 10-Gb/s NRZ data signals were generated with the delay between the two sets of signals controlled by the mainframe. By varying the delay, the phase detector characteristic can be measured and plotted. Fig. 5 shows the DC output voltage of the PD vs. the phase error.

**Fig. 5.** Phase detector characteristic with simulated and measured results.

Fig. 5 shows that the simulated and measured results have different linearity range and output voltage levels. The measured result has much better linearity. This is due to the fact that the actual die has higher parasitic capacitances on the signal paths than the simulation models provide which compensates the higher than required gain of the master branch in Fig. 2. On the other hand, the attenuation on the input and output signals through the measurement equipment (probes, SMA cables and connectors) contributes to the reduction of output voltage levels in the measured result. This reduction of voltage levels would not affect the performance of the PD in the CDR as a charge pump or buffer can be used for voltage level sensitivity adjustments. Both the measured and simulated results have a non-zero phase offset which can be explained by the fact that the data signal propagates through a slightly longer signal path to the output node than the clock signal does. An external delay block for the PLL can be used to compensate this difference in the CDR design.

It is shown that this type of PD combines the linear characteristic and high-speed performance of the Hogge and Bang-Bang or Alexander PDs. A linear range with no dead zone on phase error from \( -\pi/2 \) to \( \pi/2 \) is shown. This design has extreme low power consumption. The fastest switching node, master branch of the PD, requires a 1 mA tail current, resulting with approximately 4.66 mA current drawn by the whole PD circuit. Therefore, the PD dissipates a total power of 14.9 mW from a +/-1.6 V supply. The power dissipation of the output drivers is not included in this calculation.

**References**

