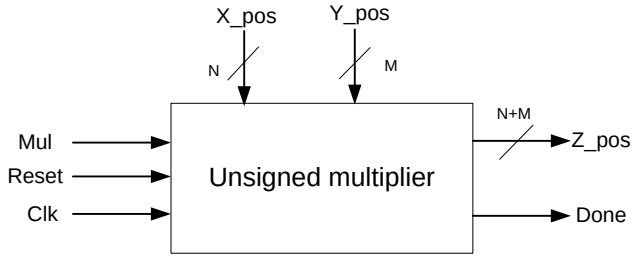
ELEC4708 Lab2

Week 2: Unsigned multiplier and Signed Multiplier

Unsigned Multiplier

The unsigned multiplier multiplies two binary integers. Multiplication can be implemented exactly the same way as with decimal numbers. Simply take each bit of the multiplier (X in this case) and if it is zero, then add nothing, but if the bit is one, add the shifted multiplicand (Y in this case). You implement this by having a partial product and then add the shifted multiplicand (or zeros) at each stage of the process until the multiplication is complete. See Weste & Harris' textbook, section 11.9.7 for further discussion.

Mul is an enable signal which signals the multiplier to begin operating. X_pos and Y_pos are the parallel signals coming from your two's complement modules. Z_pos is the parallel output of the multiplier and goes to the Z two's complement module. Done signals the completion of the multiply operation.



Test Bench

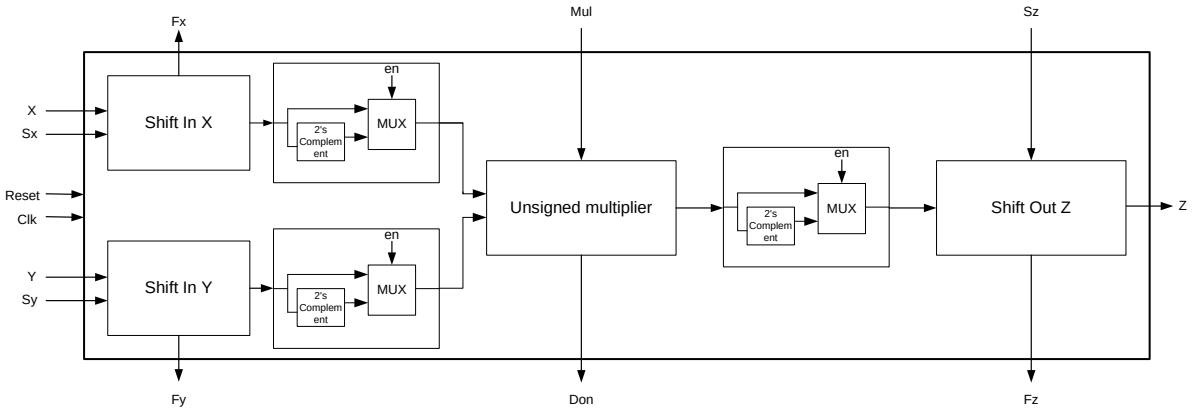
1. X=3 and Y=1
2. (Largest positive X) / 2 and (Largest positive Y) / 2
3. Largest positive X and Largest positive Y

Deliverables

- Commented Code and Test benches
- Waveforms of test bench

Signed Multiplier

The signed multiplier can use an unsigned multiplier by simply testing whether inputs are negative, carry out an unsigned multiplication, and then depending on how many of the inputs are negative, invert the output (2's complement). The method of checking for negative numbers is relatively simple, as an XOR function on the MSB of the two input signed numbers will indicate whether the output needs to have a 2's complement taken.



After testing your top module and making sure it works fine, you can go through the second tutorial for Verilog synthesis and start synthesizing your multiplier. Design Analyzer should create the schematics for your Multiplier.

Test Bench

1. 1 x -1
2. -1 x -1
3. (Largest positive X) / 2 and (Largest positive Y) / 2
4. (Largest negative X) / 2 and (Largest negative Y) / 2
5. (Largest negative X) / 2 and (Largest positive Y) / 2
6. Largest positive X and Largest positive Y
7. Largest negative X and Largest negative Y
8. Largest positive X and Largest negative Y

Deliverables

- Commented Verilog code for top module and test bench.
- Have the test bench show x_parallel, y_parallel (after shiftin) and z_parallel (before shiftout) so that they are easier to see.
- **Commented** Waveforms
- Submit the synthesized schematics for the Signed multiplier