

ELEC4708 Lab2

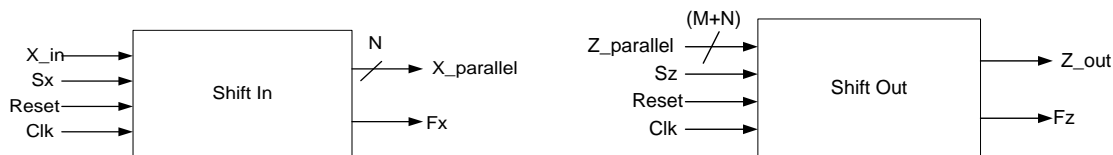
Week 1: Shift in/out and 2's complement

Please read Lab 2 instructions carefully and understand the operation and structure of the multiplier. You will design the multiplier in 4 sessions. This is the first part.

Next, perform the HDL Simulation Tutorial. You need to learn the procedure and apply it here.

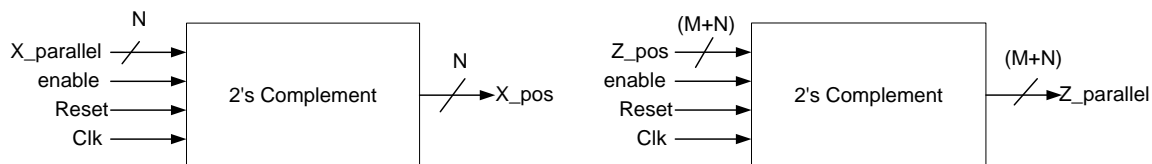
In this session we will create shift In/Out and 2's complement modules. Shift in module is used to read in the 2 inputs, X and Y and convert data from serial to parallel. Shift out module is used to output the multiplication result, Z, and convert data from parallel to serial.

The Shift In/Out module is signaled to begin the operation on the rising edge of the S{x,y,z} signal, the F{x,y,z} output signal remains low until the correct number of bits has been shifted, and then goes high. Reset is an asynchronous reset signal, which sets all outputs to low. Each shift operation takes place at the rising edge of Clk.



For a signed multiplier we need to check if the inputs are positive or negative. The most significant bit indicates the sign of the integer. To calculate the 2's complement of an integer, invert the binary equivalent of the number by changing all of the ones to zeroes and all of the zeroes to ones (also called 1's complement), and then add 1.

The Reset and Clk signals behave the same as described for the Shift modules (the use of the Clk signal is optional in the 2's complement modules). The enable signal controls whether the module outputs a two's complemented version of the input or not. When enable is low, the module can either pass the input to the output directly, or set the output to all low (whichever you choose, make sure the behaviour is consistent between all modules).



Note that the x and y 2's complement blocks have a *signed input* and an *unsigned output* while the z 2's complement block has an *unsigned input* and a *signed output*.

Test Benches

Shift-In/Out

- a) Alternating 1 and 0 (e.g. if $M = 12$, input = 101010101010)
- b) Alternating 1 and two 0's (e.g. if $M = 12$, input = 100100100100)
- c) Make sure this works for both the input and output shift registers, i.e.: results for X, Y, and Z must be shown

2's Complement

Test the following values based on your M-sized numbers.

- a) -1
- b) 1
- c) Max Value (Highest Positive Value)
- d) Min Value (Most Negative Value)
- e) Last two numbers in id * 2 (e.g. $35 * 2 = 70$, test 70)
- f) -(Last two numbers in id) * 2 (e.g. $-35 * 2 = -70$, test -70)

Deliverables

- Code for all modules and test benches
- Waveforms of all test benches