Exercises on Organization

⊙ **For a Pentium II processor descriptor that contains a base address of 00280000 H, a limit of 00010 H, and G=1, what starting and ending locations are addressed?**

⊙ **Code a descriptor that describes a memory segment that begins at location 03000000 H and ends at location 05FFFFF H. This is a data segment that grows upward in the memory system and can be written, for an 80386 Intel processor.**

- If the processor sends linear address 00200000 H to the paging mechanism, which paging directory entry is accessed and which page entry is accessed.

- What is wrong with a MOV [BX],[DI] instruction?

- What, if anything, is wrong with MOV AL, [BX][DI] instruction?

- Suppose DS=1100 H, BX=0200 H, LIST=0250 H, and SI=0500 H, determine the address accessed by each of the followin instructions.

  a) MOV LIST[SI], EDX

  b) MOV CL, LIST[BX+SI]

  c) MOV CH, [BX+SI]

⊙ Explain what happenswhen PUSH EAX instruction is executed. Assume SP=0100 H and SS=0200 H.

⊙ Develop a sequence of instructions that copy 12 bytes of data from an area of memory addressed by SOURCE into an area of memory addressed by DEST.

⊙ What is wrong with a MOV CS, AX instruction?

⊙ If AX=1001 H and DX=20FF H, list the sum and the content of each flag register bit (C, A, S, Z, and O) after the ADD AX, DX instruction executes.

⊙ What is wrong with INC[BX] instruction?

⊙ Develop a sequence of instructions that sets (to 1) the rightmost 4 bits of AX, clears (to 0) the leftmost three bits of AX, and inverts bits 7, 8, and 9 of AX.

⊙ Why are buffers required in 8086- and 8088-based systems?

⊙ What two 8086 operations occur during a bus cycle?

⊙ **Briefly describe the purpose of each T state from T1 to T4.**

⊙ **Modify the NAND gate decoder in Figure 10-13 to select the memory for address range DF800 H-DFFFF H.**

⊙ **Modify Figure 10-19 by rewriting the PAL program to address B0000 H–BFFFF H.**

⊙ **Modify the circuit of Figure 10-20 to select memory locations 68000 H–6FFFF H.**