First Midterm Exam, Fall 2000, October 23

ELE-461: Microprocessor Systems

Department of Electronics, Carleton University

Instructor: Maitham Shams
Aids: All Allowed

Name: _____
ID: _____

Write your name and ID number on all three pages. Attempt all questions. Exam marks total to 90, so you automatically get 10 bonus marks for writing the exam! Good luck.

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[1] (4 marks) Microprocessors can only exhibit a limited part of human intelligence. What particular characteristic makes them so useful then? Speed

[2] (6 marks) What type of memory *device* is mostly suitable for each of the following.

a) Small amount of data which is accessed frequently: SRAM

b) Permanent data for computer set-up: ROM / Flash / EROM

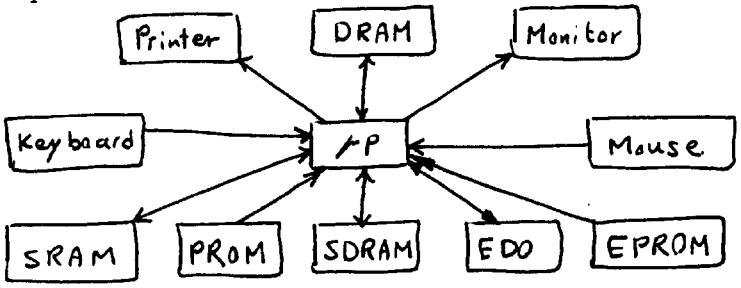
e) Very large amount of application data: DRAM

[3] (6 marks) Compatibility between the later and the earlier microprocessors has been a successful strategy for the Intel family. Give two *distinct* examples of the modifications that demonstrate this compatibility.

answer 1: Registers extended such that all bytes, words, or double words can be addressed. (e.g. AL, AH, AX, EAX all register A).

answer 2: Memory modes divided into real and protected. real mode for earlier μP compatibility.

[4] (10 marks) Draw a simple block diagram of a microprocessor and the following 10 peripherals around it: a keyboard, a printer, a DRAM, a monitor, a mouse, an SRAM, a PROM, an SDRAM, an EDO, and an EPROM. Only and only show the direction of data flow between the microprocessor and each peripheral.



[5] (7 marks) Assume DS=00EF(H). Answer the following questions regarding memory management in the real and protected modes. DS = 0000 0000 1110 1111 (TI RPL)

a) What does DS specify in the real mode? What specifications can you give?
A data segment in memory. Starts at 00EF0, with 64K limit, ends at (FFFF) 10EEE

b) What does DS specify in the protected mode? What specifications can you give?
Selector for descriptors. selector specifies descriptor number 1D = 29
it is local descripter with lowest privillege (11).

[6] (12 marks) The last stored items in the stack are the following hexadecimal values: 08 (very last), FA, 14, 92, 5E, 38, etc. Assume SS=00E0(H) and SP=01CB(H).

a) What is the physical address of the location containing 08? SSx10 + SP = 00E00 + 01CB = 00FCB

Specify the following after a POP EAX instruction is executed in the real mode.

b) Content of EAX: 92 14 FA 08

c) Content of SS: 00E0

d) Content of SP: 01CB + 4 = 01CF

e) Content of the location SP pointing to: 5E

f) Physical address SP pointing to: 00FCB + 4 = 00FCF

[7] (12 marks) Write a single *logical* instruction for each of the following operations. Note that no other changes should occur.

a) Set the most significant nibble in AX to 1: OR AX, F000

b) Clear the even-numbered bits in AX to 0: AND AX, AAAA

c) Invert bits number 0, 5, 10, and 15 in AX: XOR AX, 8421

d) Change the sign of the content of AX: NEG AX

e) Multiply the content of AX by 16: SHL AX, 4

f) Test bit number 5 in AX: TEST AX, 32

[8] (6 marks) Write a piece of code to input 150 words of data from a device whose address is PORINP and send it to another device whose address is POROUT.

Need a place in memory for storage, call it "storage" at its base.

```
MOV   DI, OFFSET STORAGE
MOV   DX, PORIN
CLD
MOV   CX, 150
REP   INSW
```

```
MOV   SI, OFFSET STORAGE
MOV   DX, POROUT
CLD
MOV   CX, 150
REP   OUTSW
```

[9] (12 marks) Indicate why each of the following are needed in relation to microprocessors.

a) Tri-state inverters: For sharing buses

b) Directives in assembly: To specify to assembler the size of data (byte, word, el

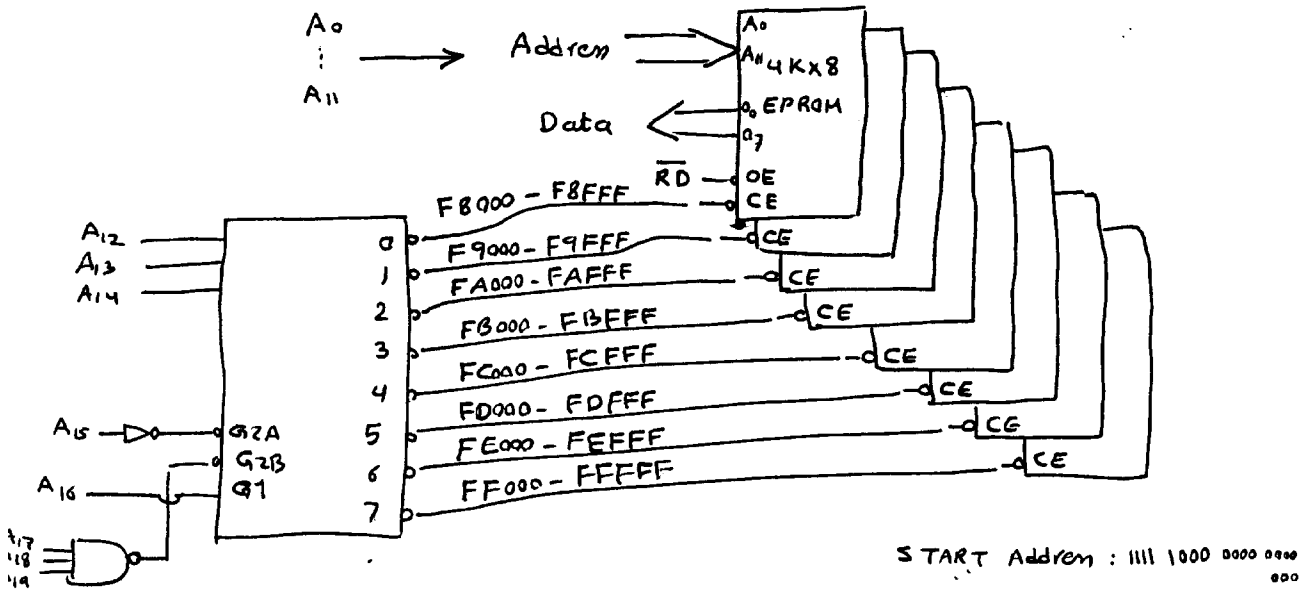
c) Wait states: To enable access / interface with slower memory / IO.

d) Buffers at outputs: To drive large loads / Fanouts.

e) Bi-directional buffers: For passing data both ways (used with data bus)

f) Clock signal: For synchronization of different operations / devices.

[10] (15 marks) For an 8080 microprocessor (i.e. 20-bit address bus and 8-bit data bus), use the decoder technique to map the upper most 32Kb of memory into eight 4K×8 EPROM chips. Draw the circuit and indicate the start and the end addresses accessible through each EPROM.



START Addres : 1111 1000 0000 0000 000

F 8 0 0 0

End Addres : F F F F F

Any Negative or Positive Comments

If you like, you may state any comments or concerns regarding the course, lectures, exam, and labs here. I really appreciate your input.

Second Midterm Exam, Fall 2000, November 27

ELE-461: Microprocessor Systems

Department of Electronics, Carleton University

Instructor: Maitham Shams
Aids: All Allowed

Name:
ID: Solution

Write your name and ID number on all three pages. Attempt all questions. You have one hour to write the exam.

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[1] (8 marks) Give two possible reasons for using an interface unit.

(4) a) Some peripherals are electromagnetic devices and need signal conversion.

(4) b) Data transfer rates of peripherals may be different than CPU.

c) Data codes and formats of peripherals may be different than CPU.

d) operation modes of peripherals differ from one another and they should not interfer each other

[2] (8 marks) In relation to interfacing a processor to a memory system with more than one bank,

a) Why a separate write control signal is needed for each bank?

(4) To enable CPU to access individual banks for writing data as byte, word, or double-word.

b) Why only one read control signal is needed for all banks?

(4) CPU reads only the portion that it needs from the bus. It may read a byte, a word, or a double word.

[3] (16 marks) Evaluate the Hamming Code parity bits for the following n-bit data and write down the $n + k$ words.

a) 110 $n=3 \Rightarrow k=3$ $P_1\ P_2\ D_3\ P_4\ D_5\ D_6$ (1)

(2) $P_1 = xor(3,5) = 0$ (2) $P_4 = xor(5,6) = 1$ } 0 1 1 1 1 0

(2) $P_2 = xor(3,6) = 1$

b) 0110101 $n=7 \Rightarrow k=4$ $P_1\ P_2\ \overset{0}{D_3}\ P_4\ \overset{1}{D_5}\ \overset{1}{D_6}\ \overset{0}{D_7}\ P_8\ \overset{1}{D_9}\ \overset{0}{D_{10}}\ \overset{1}{D_{11}}$

(2) $P_1 = xor(3,5,7,9,11) = 1$ (2) $P_4 = xor(5,6,7) = 0$ } 1 0 0 0 1 1 0 0 1 0 1

(2) $P_2 = xor(3,6,7,10,11) = 0$ (2) $P_8 = xor(9,10,11) = 0$ (1)

[4] (8 marks) Mention two reasons for preferring asynchronous date transfer over synchronous.

(4) a) Asynchronous method adopts the advent of technologies (scales better with technology)

(4) b) Asynchronous method allows use of a wider variety of devices

[5] (8 marks) Answer the following questions regarding signal bouncing.

(4) a) What sort of danger it poses? wrong data may be sampled.

(2) b) What is the hardware technique for debouncing? using special switches called debouncing switches.

(2) c) What is the software technique for debouncing? Delay Loop insertion before sampling

[6] (8 marks) Define the following terms, give their units, and mention an equivalent term for each.

a) Latency (2) - Time taken to finish an operation
(1) - seconds or ns
(1) - response time

b) Throughput (2) - Amount of data processed per second
(1) - bytes/sec or Kb/sec or Mb/sec
(1) - Bandwidth

[7] (14 marks) An I/O device uses a 32-bit bus to transfer data to a 1.2 Ghz CPU at a rate of 100 KB per second. In each access, 64 bytes of data are transferred. If a polling operation for this device takes 500 ns, calculate the overhead of the polling technique as the fraction of CPU time consumed.

(4) Polling operation takes $500\text{ ns} \times 1.2 \frac{10^9 \text{ cycles}}{\text{sec}} = 600$ cycles

(4) CPU must poll at rate of $\frac{100 \frac{KB}{sec}}{64 \frac{\text{bytes}}{\text{access}}} = 1562.5$ times/sec $\simeq 1563$

(3) Cycles per second for polling $= 1563 \times 600 = 937800$

(3) Fraction of CPU time consumed $= \frac{937800}{1.2 \times 10^9} = 0.07815\% \simeq 0.08\%$

[8] (30 marks) For an 80386SX microprocessor (i.e. 24-bit address bus and 16-bit data bus), use the PAL technique to map the lower most 0.5Mb of memory into eight 64K×8 SRAM chips. The processor provides MRDC, MWTC, BHE, and BLE (i.e. A0) control signals. The SRAM chips have WE, OE, and CE control inputs. Draw a simple circuit diagram, label the wires, and write the expressions needed for programming the PAL. Use a simple box for the PAL and identify its input and output signals.

See the back.

Any Negative or Positive Comments

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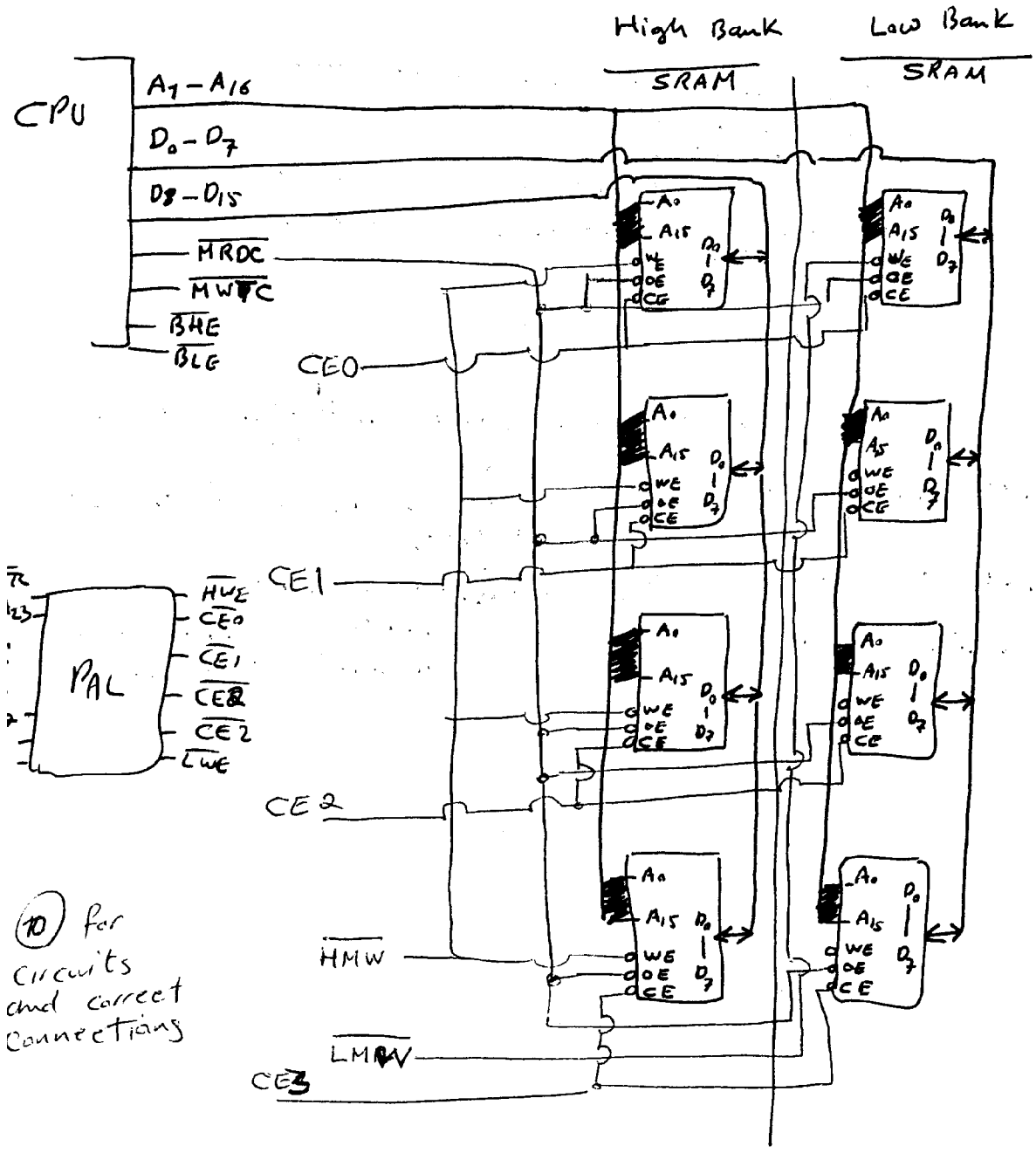

(10) for circuits and correct connections

(2) $\overline{HWE} = \overline{BHE} \cdot \overline{MWTC}$

(2) $\overline{LWE} = \overline{BLE} \cdot \overline{MWTC} = \overline{A_0} \cdot \overline{MWTC}$

(4) $\overline{CE0} = \overline{A_{23}} \cdot \overline{A_{22}} \cdot \overline{A_{21}} \cdot \overline{A_{22}}\ \overline{A_{21}}\ \overline{A_{20}}\ \overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}}$

(4) $\overline{CE1} = (\quad = \quad) \cdot \overline{A_{18}} \cdot A_{17}$

(4) $\overline{CE2} = (\quad = \quad) \cdot A_{18} \cdot \overline{A_{17}}$

(4) $\overline{CE3} = (\quad = \quad) \cdot A_{18} \cdot A_{17}$