Name & ID: ✱ { $P_1 = D_3 \oplus D_5 \oplus D_7$; $P_2 = D_3 \oplus D_6 \oplus D_7$; $P_4 = D_5 \oplus D_6 + D_7$ } $P_8 = D_4 \oplus D_1$

[3] (20 marks)

[3A] (10+5=15 marks) A modified single-error correcting, double-error detecting Ha four bits of Data D_3, D_5, D_6, and D_7 has the following parity bit equations: P_1 = $P_2 = D_3 \oplus D_5 \oplus D_7$, $P_4 = D_3 \oplus D_6 \oplus D_7$, and $P_8 = D_5 \oplus D_6 \oplus D_7$.

a) Find the binary values of the four check bits for a single error in each of the eight bi code. Form a table.

$C_1 = P_1 \oplus D_3 \oplus D_5 \oplus D_6$ (1)
$C_2 = P_2 \oplus D_3 \oplus D_5 \oplus D_7$ (1)
$C_4 = P_4 \oplus D_3 \oplus D_6 \oplus D_7$ (1)
$C_8 = P_8 \oplus D_5 \oplus D_6 \oplus D_7$ (1)

Error Bit		C_8	C_4	C_2	C_1	
1		0	0	0	1	(0.5)
2		0	0	1	0	(0.5)
3		0	1	1	1	(1)
4		0	1	0	0	(0.5)
5		1	0	1	1	(1)
6		1	1	0	1	(1)
7		1	1	1	0	(1)
8		1	0	0	0	(0.5)

P_1 P_2 D_3 P_4 D_5 D_6 D_7 P_8

b) For each of the following words read from memory evaluate the check bits and indicate error, double error, or no error has occured. Write the correct word were possible.

i) 10100011

$C_8\ C_4\ C_2\ C_1 = 0000$ ⇒ No error (1)

ii) 11001110

$C_8\ C_4\ C_2\ C_1 = 1011$ ⇒ error in bit 5 (1)

Right word is : 11000110 (1)

iii) 00011101

$C_8\ C_4\ C_2\ C_1 = 1010$ (1) ⇒ double error (1)

Since it is not in the above.

[3B] (3 marks) What are the limitations of the following techniques for detecting and in memory systems? (0.5 each)

a) Error detection using single parity — one bit

b) Error correction using single parity — none

c) Error detection using basic Hamming Code — one bit

Name & ID: ....

[4] (6+5+4=15 marks) We are interested in two implementations of a machine, one witl special floating-point hardware. Both machines have a clock rate of 1000 MHz. Consi with the following mix of operations.

floating-point multiply	10%	30%
floating-point add	15%	
floating-point divide	5%	
integer instructions	70%	

Machine MFP (Machine with Floating Point) has floating point hardware and can th the floating point instructions directly. It requires the following number of clock cycles fc class.

floating-point multiply	6
floating-point add	4
floating-point divide	20
integer instructions	2

Machine MNFP (Machine Without Floating Point) has no floating-point hardware anc the floating-point operations using integer instructions. The integer instructions all ta The number of integer instructions needed to implement each of the floating-point opera

floating-point multiply	30
floating-point add	20
floating-point divide	50

a)Find the MIPS ratings for both machines. $MIPS = \frac{Inst\ Count}{Exec\_time \cdot 10^6} = \frac{Inst\ C}{Inst\ C}$

$MIPS = \frac{clock\ rate}{CPI \times 10^6}$

Are

CPI for MFP = $(10 \times 6 + 15 \times 4 + 5 \times 20 + 70 \times 2)/100 = 3.6$ (2)

CPI for MNFP = 2 (1)

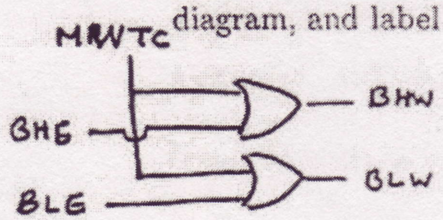
MIPS for MFP = $\frac{1000M}{3.6 \cdot 10^6} = 278$ (1) and MIPS for MNFP = $\frac{1000}{2 \cdot 10}$

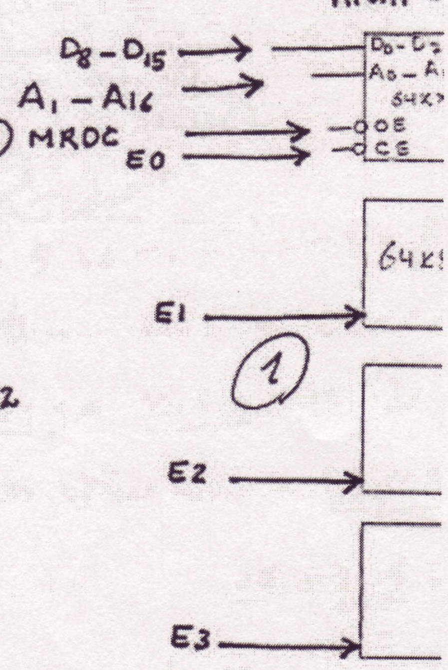
b)If the machine MFP needs 300 million instructions for this program, how many intege the machine MNFP require for the same program?

Instruction Class	Frequency on MFP	Count on MFP $\times 10^6$	Count on MN
Floating Point Multiply	10%	30	900
Floating Point Add	15%	40	900

Name & ID: ....

[5] (20 marks) A computer system with an 80386SX microprocessor (24-bit address bu bus) requires 4 Mb of memory starting at address 0_H. This 4 Mb should be divided into at the bottom, 2.0 Mb of DRAM at the middle, and 0.5 Mb of EPROM at the top. T are 64K×8 EPROM chips, 128K×8 SRAM chips, 512K×4 DRAM chips, 3 × 8 decoder and combinational logic gates. The processor provides MRDC, MWTC, BHE, and BLE signals. The SRAM and DRAM chips have WE, OE, and CE control inputs. The EPRC and CE control inputs. Find the start and end addresses for the three memory parts, dra diagram, and label the wires in your design.





EPROM : 0.5 Mb/64K = 8

$0.5\ Mb = 2^{19} = [2^{16} \times 4]\ 2$

DRAM : $[(512\ K \times 4)\ 2] \times 4 = 2.0\ Mb = 2^{21} = [2^{19} \times 2]\ 2$

SRAM : 1.5 Mb/128 Kb = 12

$1.5\ M = [6 \times 2^{17}]\ 2$

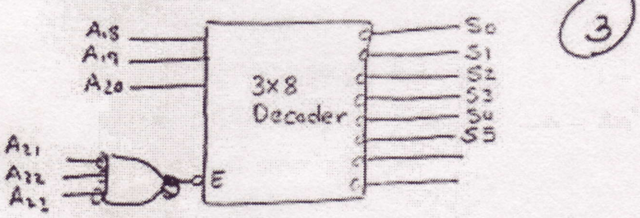
SRAM: 000000 — 17FFFF (2)

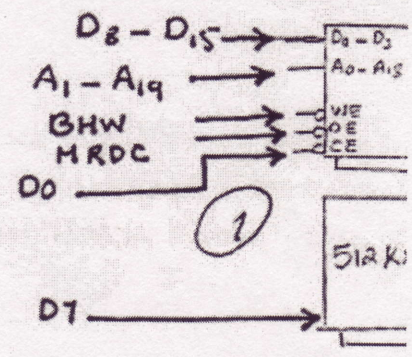
A20 A19 A18 A17 ... A1

0000 0000 0000 0000 0000 0000

0001 0111 1111 1111 1111 1111

fixed — variable — don't care





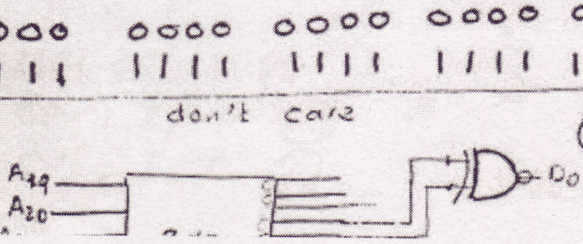
DRAM : 180000 — 37FFFF (2)

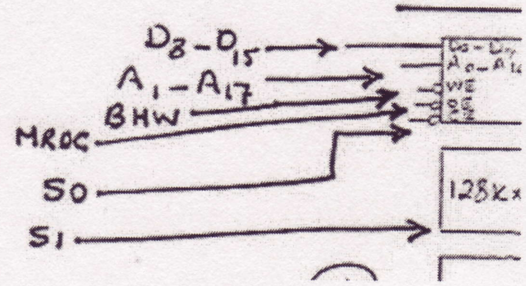
A19 ... A1

001 1000 0000 0000 0000 0000

011 0111 1111 1111 1111 1111

fixed — variable — don't care





Name & ID: ....

[6] (20 marks)

[6A] (10 marks) A program repeatedly performs a three-step process: It reads in a 4 Kb
disk, does some processing on that data, and then writes out the result as another 4 K
on the disk. Each block is located on a single track on the disk. The disk rotates at 5
average seek time of 8 ms, and has a transfer rate of 20 Mb/sec. The controller overhead
program is using the disk or processor, and there is no overlapping of disk operation wit
processing step takes 20 million clock cycles, and the clock rate is 400 MHz. What is the
speed of the system in blocks processed per second.

Average rotation time = $\dfrac{0.5 \text{ rotations}}{5400 \frac{\text{rotations}}{\text{minute}} \cdot \frac{\text{minute}}{60 \text{ seconds}}}$ = 5.56 r

Transfer time = $\dfrac{4 \text{ Kb}}{20 \text{ Mb/sec}}$ = 0.2 ms (2)

⇒ Average disk access time = 8 ms + 5.56 ms + 0.2 ms + 2

Since each block processed involves two accesses (read

disk component of time is 2X15.76 = 31.52 ms (1)

Computation takes 20 million cycles X 1/400 MHZ = 50 ms

Thus, total time to process one block is 50 + 31.5?

Number of block processed per second is

1/0.08152 = 12.27 (1)

[6B] (6 marks) For the following set of variables, {CPI, clock rate (F), cycle time (T),
instructions in program (I), number of cycles in program (C)}, identify all of the subsets
to calculate execution time. Each subset should be minimal; that is, it should not co
that is not needed.

freq

CPI ≡ average cl

a) F, C (1)

b) T, C (1)

c) MIPS, I (1)

d) CPI, C, MIPS (1)

e) CPI, I, F (1)

f) CPI, I, T (1)