Final Exam

Tuesday, 10 December, Fall 2002

97.461: Microprocessor Systems

Department of Electrical and Computer Engineering, Carleton University

Instructor:	Maitham Shams	**Exam Duration:**	3 hours
Booklets:	None	**Number of Pages:**	8
Aids Allowed:	Open Book	**Number of Students:**	125

Last Name: _____

First Name: _____

ID: _____

Write your name and ID number on all pages. Attempt all questions. In favour of fairness, I won't answer any questions. Make necessary assumptions. Wish you Good Luck.

1	2	3	4	5	6	7	Total
/6	/10	/20	/14	/20	/20	/10	/100

---

[1] (6 marks, 2 each part) **I/O Theory**

a) *compare* the following pair of concepts by their definitions, b) mention one *advantage* of the first with respect to the second and, c) mention one *advantage* of the second with respect to the first one.

Comparitive Definition	Advantage of 1st	Advantage of 2nd
Polling & Interrupt-Driven I/O Communication		
Serial & Parallel I/O Communication		
Isolated & Memory-Mapped I/O System		

[2] (10 marks, 1 each part) **Terminology** Briefly *explain* the following terms and concepts.

a	Granularity Bit	
b	Refresh Cycle	
c	Half- Duplex	
d	DMA	
e	Handshaking	
f	Interface Unit	
g	EEPROM	
h	Descriptor	
i	Interrupt Mask	
j	Opcode	

[3] (20 marks) **Error Detection and Correction**

[3A] (10+5=15 marks) A *modified* single-error correcting, double-error detecting Hamming code for four bits of Data D_3, D_5, D_6, and D_7 has the following parity bit equations: $P_1 = D_3 \oplus D_5 \oplus D_6$, $P_2 = D_3 \oplus D_5 \oplus D_7$, $P_4 = D_3 \oplus D_6 \oplus D_7$, and $P_8 = D_5 \oplus D_6 \oplus D_7$.

a) Find the binary values of the four check bits for a single error in each of the eight bit positions of the code. Form a table.

bUsing the results of part b, for each of the following words read from memory evaluate the check bits and indicate whether a single error, double error, or no error has occurred. Write the correct word were possible.

i) 10100011

ii) 11001110

iii) 00011101

[3B] (3 marks) What are the limitations of the following techniques for detecting and correcting errors in memory systems?

a) Error detection using single parity

b) Error correction using single parity

c) Error detection using basic Hamming Code

d) Error correction using basic Hamming Code

e) Error detection using Hamming Code plus a parity bit

f) Error correction using Hamming Code plus a parity bit

[3C] (2 marks) How much memory do you need for implementing the basic hamming code technique for a 64K×8 DRAM chip? Why?

[4] (5+5+4=14 marks) **Computer Performance**

We are interested in two implementations of a machine, one with and one without special floating-point hardware. Both machines have a clock rate of 1000 MHz. Consider a program P, with the following mix of operations.

floating-point multiply	10%
floating-point add	15%
floating-point divide	5%
integer instructions	70%

Machine MFP (Machine with Floating Point) has floating point hardware and can therefore implement the floating point instructions directly. It requires the following number of clock cycles for each instruction class.

floating-point multiply	6
floating-point add	4
floating-point divide	20
integer instructions	2

Machine MNFP (Machine Without Floating Point) has no floating-point hardware and so must emulate the floating-point operations using integer instructions. The integer instructions all take 2 clock cycles. The number of integer instructions needed to implement each of the floating-point operations is as follows.

floating-point multiply	30
floating-point add	20
floating-point divide	50

a)Find the MIPS ratings for both machines.

b)If the machine MFP needs 300 million instructions for this program, how many integer instructions does the machine MNFP require for the same program?

c) Considering the instructions counts from part (b), find the executions time for the program on MFP and MNFP.

[5] (20 marks) **Memory Design**

A computer system with an 80386SX microprocessor (24-bit address bus and 16-bit data bus) requires 4 MB of memory starting at (the bottom) address 0_H. This 4 MB should be divided into 1.5 MB of SRAM at the bottom, 2.0 MB of DRAM at the middle, and 0.5 MB of EPROM at the top. The available parts are 64K×8 EPROM chips, 128K×8 SRAM chips, 512K×4 DRAM chips, 3×8 decoders, 2×4 decoders, and combinational logic gates. The processor provides $\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{BHE}}$, and $\overline{\text{BLE}}$ (i.e. A0) control signals. The SRAM and DRAM chips have $\overline{\text{WE}}$, $\overline{\text{OE}}$, and $\overline{\text{CE}}$ control inputs. The EPROM chips have OE and CE control inputs. Find the start and end addresses for the three memory parts, draw a simple circuit diagram, and label the wires in your design. Do all calculations in this page and draw the circuit in the next page.

Circuit Diagram for [5]

[6] (20 marks) **Miscellaneous**

[6A] (10 marks) A program repeatedly performs a three-step process: It reads in a 4 Kb of data from hard disk, does some processing on that data, and then writes out the result as another 4 Kb block elsewhere on the disk. Each block is located on a single track on the disk. The disk rotates at 5400 RPM, has an average seek time of 8 ms, and has a transfer rate of 20 Mb/sec. The controller overhead is 2 ms. No other program is using the disk or processor, and there is no overlapping of disk operation with processing. The processing step takes 20 million clock cycles, and the clock rate is 400 MHz. What is the overall (average) speed of the system in blocks processed per second.

[6B] (6 marks) For the following set of variables, {CPI, clock rate (F), cycle time (T), MIPS, number of instructions in program (I), number of cycles in program (C)}, identify all of the subsets that can be used to calculate execution time. Each subset should be minimal; that is, it should not contain any variable that is not needed.

a)
b)
c)
d)
e)
f)

[6C] (4 marks) List four *distinct* differences between the architectures of Intel 8086 and Motorola 68000 microprocessors.

a)
b)
c)
d)

[7] (10 marks) **Short-Answer Questions**

Answer the following questions.

a) (1 mark) In what case DMA overhead is small compared to that of interrupt-driven I/O?

b) (2 marks) Why MIPS is not a good measure of performance?

c) (2 marks) How is an interrupt different than a processor exception?

d) (1 mark) Can one invert BHE signal to get BLE? why?

e) (2 marks) In what way(s) PROM is different than PAL?

f) (2 marks) Why in some microprocessors address and data lines are internally multiplexed? Why do we need to demultiplex them out of the microprocessor?