**ENEL5808** **Student Name** _____
**Signal Processing Electronics**
**Mid-Term Examination** **Student Number** _____

Oct. 25,2007 7:30PM - 9:00PM R. Mason
answer all questions on sheet provided

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1. (5 points) Multiple Choice, Circle BEST answer

(a) Thin film resistors are generally better than implanted resistors because:
- (i) they have a higher temperature coefficient
- (ii) they have a wider range of values
- (iii) they are easier to make
- (iv) they provide higher yield

(b) Large IC capacitors are made up of a number of smaller unit size capacitors to:
- (i) reduce the area of the capacitor
- (ii) reduce the paracitics of the capacitor
- (iii) improve the matching of capacitors
- (iv) reduce the plate resistance of the capacitor

(c) A circuit designer can increase the $g_m$ of a NMOS transistor by:
- (i) increasing the carrier mobility
- (ii) increasing the threshold voltage
- (iii) increasing the width
- (iv) decreasing the drain current

(d) The main advantage of a cascode current source is:
- (i) smaller output swing
- (ii) higher output impedance
- (iii) more transistors
- (iv) better device matching

(e) What is the typical voltage gain of a standard telescopic cascode CMOS amplifier?
- (i) 10 dB
- (ii) 20 dB
- (iii) 60 dB
- (iv) 120 dB

2. (10 points) Short Answer

(a) What are the advantages of a telescopic cascode amplifier compared to a folded cascode amplifer?

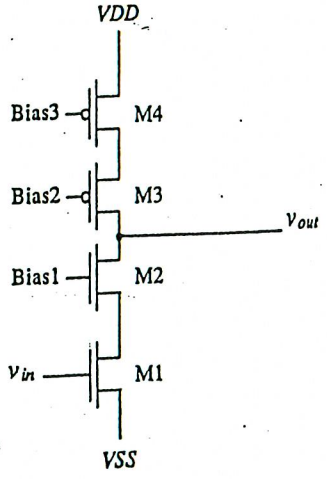
(b) Draw the layout cross section of a CMOS inverter, including substrate contacts and show any paracitic bipolar transistors.

(c) List in order the layers that are applied/added in a 5 metal layers CMOS process. Why is the device well layer applied before the drain/source implants?

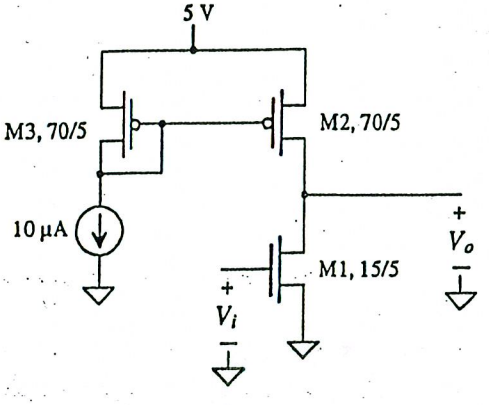
(d) A basic nmos differential pair with resistive loads has a maximum single sided output slew rate of 25 V/us into a 0.5 pF load. What do we know about the bias currents in the circuit? How can we increase the slew rate?

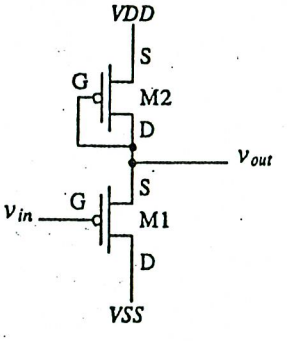
(e) Why do we use dummy cells in analog circuit layouts? Draw an example layout with a dummy cell (don't forget the correct voltages on the dummy cell).

3. (5 points) For the following circuit W/L for all transistors is 100um/1.5um, $u_nC_{ox}$ = 80 uA/V², $u_pC_{ox}$ = 25uA/V², $I_{bias}$ = 100uA, $r_{ds\text{-}p}$ (ohms) = $r_{ds\text{-}n}$ (ohms) = 6,000L (um)/$I_d$ (mA). Ignoring the body effect, what is the gain of this stage?




4. (5 points) Draw and label the DC transfer function (Vout vs. Vin) for the following circuits. Explain the purpose of $M_1$, $M_2$ and $M_3$ for each circuit. What kind of circuits are these normally referred to as?



5. (5 points) What is the following circuit? Explain the purpose of each transistor.