ELEC5808 **Assignment 2** Due: Oct. 15/2014

1. Using Cadence and 90nm technology create an equivalent layout for the CMOS differential pair circuit you designed in assignment1. Make sure the layout is DRC clean (note: you do not have to layout the load capacitance or current source)

2. Extract and LVS the differential pair layout to make sure it is equivalent to the schematic

3. Perform a transient simulation of the extracted layouts and compare to the transient simulations of the schematic.

Submit layout, extraction and LVS logs showing no errors, simulations results including a table comparing layout and schematic results.