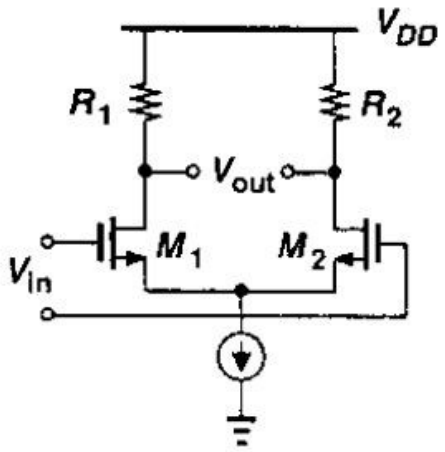
ELEC5808 Assignment 1 Due: Oct. 1/2014

1. Using Cadence and 90nm technology create a CMOS differential pair circuit with resistive load (see below) using a 1.2V power supply, a 100uA current source, and a load capacitance of 0.1 pF across the output.



2. Plot the dc transfer function (vout vs. vin) of the differential pair. Adjust the transistor and/or resistor sizes to give a DC gain of between 8-12.

3. Perform a transient simulation and determine the rise time, fall time and delay of the differential pair. Assume the input waveform is a 10mVpp square wave with a common mode DC bias of 0.6V and has a 100ps risetime and falltime. Try to optimize the differential pair circuit (by changing transistor lengths and widths and load resistor values) so that the output rise time and fall time are less than 10nS while maintaining a gain of 8-12.

4. Measure the power dissipation of the differential pair (include the power dissipation of the input signal power supplies) assuming the input square wave of question #3 has a frequency of 10MHz. Resize the transistor to maintain the 10nS rise and fall times and gain while minimizing the power dissipation. Explain how you did this.

Submit schematic and simulation results and any analysis you performed.