Field Programmable Gate Array (FPGA) Devices
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  • FPGAs with embedded processors
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  • APEX FPGAs
  • Stratix FPGAs
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➢ Xilinx FPGAs and CPLDs
  • CPLDs
  • Virtex–I, II FPGAs
  • Spartan FPGAs
  • Virtex–5 FPGAs
Altera CPLDs

- CPLDs
  - MAX 3000
  - MAX 7000 CPLDs
  - MAX 7000AE CPLDs
  - MAX 7000B CPLDs
  - MAX 7000S CPLDs

- Comparison of MAX device propagation delays and supply voltages
Altera FPGAs with Embedded Processors

- Altera’s Excalibur devices feature an ARM processor-based embedded subsystem, or stripe, which also contains dual-port and single-port SRAM memory, memory interfaces, and peripherals.

- The integrated SDRAM controller supports SDR or DDR SDRAM at up to 133 MHz or 266 MHz, respectively, while the Excalibur device supports up to 512Mb of SDRAM.
Altera FPGAs

➢ **ADEX FPGAs**
  • Range from 576 to 4,992 LEs. Operating at 2.5V, ADEX devices are fully 64-bit, 66MHz PCI compliant and feature embedded dual-port RAM

➢ **Cyclone I FPGAs**
  • Built in a cost-optimized, all-copper 1.5V SRAM process. Up to 20,060 LEs and 288 Kb of on-chip RAM. Priced at less than US$1.50 per 1,000 LEs

➢ **APEX FPGAs**
  • High density of 1,200 to 67,200 LEs and data transfer rates up to 1Gb/s per channel. Designed to be 64-bit, 66MHz PCI compliant
Altera FPGAs

Cyclone II FPGAs

- 90 nm process with 1.2V core voltage
- Up to 68,416 LEs, 1.1Mbits of M4K Memory, 150 18x18 multipliers for DSP functions and 622 I/Os
- Support for SDR, DDR, DDR2 and QDRII SRAM up to 668 Mbps
- Support for differential LVDS, LVPECL, SSTL and HSTL I/Os
- Support for single ended LVTTL, LVCMOS, SSTL, HSTL, PCI and PCI-X
- Up to 4 programmable PLLs and 16 global clock lines
- NiosII Embedded Processor
- On-Chip Termination
## Cyclone II Family of FPGAs

<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>Logic Elements</td>
<td>4,608</td>
<td>8,256</td>
<td>14,448</td>
<td>18,752</td>
<td>33,216</td>
<td>50,528</td>
<td>68,416</td>
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<tr>
<td>M4K RAM Blocks</td>
<td>26</td>
<td>36</td>
<td>52</td>
<td>52</td>
<td>105</td>
<td>129</td>
<td>250</td>
</tr>
<tr>
<td>(4 kbits + 512 Parity Bits)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Total RAM Bits</td>
<td>119,808</td>
<td>165,880</td>
<td>239,616</td>
<td>239,616</td>
<td>483,840</td>
<td>594,432</td>
<td>1,152,000</td>
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<tr>
<td>Embedded 18x18 Multipliers</td>
<td>13</td>
<td>18</td>
<td>26</td>
<td>26</td>
<td>35</td>
<td>86</td>
<td>150</td>
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<tr>
<td>PLLs</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Differential Channels</td>
<td>58</td>
<td>77</td>
<td>132</td>
<td>132</td>
<td>205</td>
<td>193</td>
<td>262</td>
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</table>
Cyclone II Device Block Diagram
Cyclone II LE
Cyclone II LAB Structure
Cyclone II PLLs
Cyclone II I/Os
Altera Stratix FPGAs

- Stratix FPGAs
  - based on a 1.5V 0.13um, all-layer-copper SRAM process
  - Density ranges from 10,570 to 79,040 LEs
  - The integration of the 512Kb M-RAM blocks with hundreds of smaller M512 and M4K blocks provides a large on-chip memory (see figure on the next slide) or high-memory bandwidth
  - Up to 7Mb of RAM. Up to 22 DSPs. Up to 152 high-speed differential I/O channels. As many as 12 PLLs, and up to 40 system clocks
Altera Statix FPGAs

- TriMatrix memory structure

### More Bits for Larger Memory Buffering
- **M512 Blocks**
  - 512 bits per block + parity
  - Up to 767 blocks

- **M4K Blocks**
  - 4 Kbits per block + parity
  - Up to 364 blocks

- **M-RAM Blocks**
  - 512 Kbits per block + parity
  - Up to 9 blocks

### More Data Ports for Greater Memory Bandwidth
- **Applications**
  - Rake receiver correlator
  - Shift register
  - Small FIFO buffers
  - Finite impulse response (FIR) filter delay line
  - ATM cell packet processing
  - Header/cell storage
  - Channelized functions
  - Program memory for processors
  - IP packet buffering
  - System cache
  - Video frame buffers
  - Echo canceller data storage
  - Processor code storage
Altera Stratix FPGAs

Stratix GX FPGAs

- built in a 1.5V 0.13um, all-layer-copper SRAM process
- Density ranges from 10,570 to 41,250 LEs
- Up to 3.3Mb of embedded RAM with the TriMatrix memory structure. Up to 14 DSPs. Up to 8 PLLS
- With up to 20 full-duplex transceiver channels operating at up to 3.125 gigabits per second (Gbps) per channel, Stratix GX devices address the needs for high-speed backplane and chip-to-chip communications. In addition, Stratix GX devices feature embedded equalization circuitry, very low power consumption per channel, and 40" FR4 backplane drive capability.
Altera Stratix FPGAs

Stratix GX FPGAs cont.
- Up to 45 receiver and 45 transmitter high-speed differential I/O channels, each running at up to 1Gb/s
- Dynamic Phase Alignment for Accelerated Source-Synchronous Signaling
  - Source-synchronous I/O channels capable of 1-Gbps performance balance data transfer through the device. These channels, located on the opposite side of the device from the transceiver blocks, enable users to move data on and off the device using the LVDS, HyperTransport™, or LVPECL I/O standards across multiple channels
  - Each channel is equipped with embedded SERDES technology to simplify design implementation
- High-bandwidth DSP blocks for signal processing-intensive applications
- Stratix GX devices are supported in the Quartus® II software and all major third-party synthesis & simulation tools available today for implementing multi-gigabit designs.
Altera Stratix II, III FPGAs

Stratix II, III FPGAs
- Stratix II – 90nm, Stratix III - 65 nm TSMC technology
- Devices Optimized for Applications
  - L (Logic)
  - E (DSP and Memory)
  - GX (Multi-Gigabit transceivers)
- Programmable Power Consumption

![Standard FPGA](image1)

![Stratix III FPGA with Programmable Power Tachnology](image2)
# Altera Statix II, III FPGAs

## Feature Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>Stratix II (90 nm)</th>
<th>Virtex-5 (65 nm)</th>
<th>Stratix III (65 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Internal Clock Speed</td>
<td>500 MHz</td>
<td>550 MHz</td>
<td>600 MHz</td>
</tr>
<tr>
<td>On-Chip RAM</td>
<td>500 MHz</td>
<td>550 MHz</td>
<td>600 MHz</td>
</tr>
<tr>
<td>Digital Signal Processing (DSP) Block</td>
<td>450 MHz</td>
<td>550 MHz</td>
<td>550 MHz</td>
</tr>
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</table>

## Stratix III – Capacity Limits

<table>
<thead>
<tr>
<th>Feature</th>
<th>Stratix II (90 nm)</th>
<th>Stratix III (65 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adaptive Logic Modules (ALMs)</td>
<td>135,200</td>
<td></td>
</tr>
<tr>
<td>Equivalent Logic Elements (LEs)</td>
<td>338,000</td>
<td></td>
</tr>
<tr>
<td>Registers</td>
<td>270,400</td>
<td></td>
</tr>
<tr>
<td>M9K Memory Blocks</td>
<td>1,144</td>
<td></td>
</tr>
<tr>
<td>M144K Memory Blocks</td>
<td>48</td>
<td></td>
</tr>
<tr>
<td>Embedded Memory (Kbits)</td>
<td>17,208</td>
<td></td>
</tr>
<tr>
<td>MLAB (Kbits)</td>
<td>4,225</td>
<td></td>
</tr>
<tr>
<td>18x18 Multipliers</td>
<td>576</td>
<td></td>
</tr>
<tr>
<td>F1760</td>
<td>1,104</td>
<td></td>
</tr>
</tbody>
</table>

## Interconnect

<table>
<thead>
<tr>
<th>Interconnect</th>
<th>Stratix II (90 nm)</th>
<th>Virtex-5 (65 nm)</th>
<th>Stratix III (65 nm)</th>
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<tbody>
<tr>
<td>DDR2</td>
<td>333 MHz</td>
<td>333 MHz</td>
<td>400 MHz</td>
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<tr>
<td>DDR3</td>
<td>Not Supported</td>
<td>Not Supported</td>
<td>400+ MHz</td>
</tr>
<tr>
<td>QDR II</td>
<td>300 MHz</td>
<td>300 MHz</td>
<td>350 MHz</td>
</tr>
<tr>
<td>QDR II+</td>
<td>Not Supported</td>
<td>Not Supported</td>
<td>400 MHz</td>
</tr>
<tr>
<td>RLDRAM II</td>
<td>300 MHz</td>
<td>300 MHz</td>
<td>400 MHz</td>
</tr>
<tr>
<td>LVDS</td>
<td>1.25 Gbps dynamic phase alignment (DPA)</td>
<td>1.25 Gbps</td>
<td>1.25 Gbps</td>
</tr>
</tbody>
</table>
Xilinx CPLDs

- **CoolRunner–II**
  100% digital core, up to 333MHz performance, and less than 100uA of standby current, pin-to-pin (\(t_{pd}\)) speeds of 5ns

- **CoolRunner XPLA3**
  Pin-to-pin speeds of 5ns. Deliver power that is less than 100uA (standby)
Xilinx FPGAs

Virtex-II Pro FPGAs

- Consists of 10 members, each with 4 to 24 multi-gigabit transceivers; 3.1 to 125k Logic Cells
- 0.2 to 10Mbit memory
- 18 by 18 multipliers: 12 to 556
- Each multi-gigabit channel can provide a data rate of from 622Mb/s to 3.125Gb/s (baud rate)
- Each channel can also propagate a signal 40 inches at 3.125Gb/s over FR4
- Each of the larger Virtex-II Pro devices incorporates one to four PowerPC 405 processor cores
Xilinx FPGAs

- **Virtex-II Pro Applications**
  - Network Processing
  - Protocol Bridges
  - SOC design

- **Virtex-II Pro IP Block**
  - Power PC
  - Processor IP
  - Crossbar Switch
  - UART
  - FEC
  - FIR
  - Turbo Coding
  - FFT
Xilinx FPGAs

- **Virtex-II**
  - One million gates
  - Power PC
  - 3.125Gbps interfaces

- **Spartan-IIIE**
  - 19 I/O standards
  - IP (including DSP and processor cores)
  - RAM
  - digital DLL
Xilinx FPGAs

**Virtex-5**

- 1V – 65nm process
- 6 input LUTs for reduced logic stages
- 36Kbyte RAM blocks
- Low Power 0.1 - 3.2 Gbps Rocket IO
- 550 MHz DSP functions
- LX versions optimized for logic
- LXT versions optimized for serial IO
- Up to 330,000 LE and 1200 I/Os