Field Programmable Gate Array (FPGA) Design
Design Process

Design
(Graphical or HDL entry)

Compilation
(Compiler)

Simulation
(Timing diagram or analysis)

Verification
(DE2 board)

Graphical Entry

Compiler

Timing Diagram

Program CPLD

HDL Entry

Timing Analysis

Development Board
Definitions

• Logic Gate – discrete component performing a single logic function (i.e. 7400)
• PLD – a programmable device allowing functionality of several to few tens of devices
• GA – Gate Array, prefabricated, regular layout collections of transistor clusters allowing building complex logic functions through adding top metal layers (half-finished IC)
• FPGA – as above but allowing hundreds to hundreds of thousands devices
Definitions (cont.)

- Custom (Digital) IC – an IC put together by digital designers gate by gate; standard cells may be used
- ASIC – a digital circuit created fully by silicon compiler (synthesis tool); most of the layout is automated as well; often includes specialized blocks
- Structured ASIC – either standard cell ASIC with macro cells or FPGA with large IP blocks
Discrete LOGIC, PLD, FPGA
ASIC, DSP and FPGA

Performance

Cost
ASICS

- Standard-cell based design (synthesis)
- Physical layout (P&R) and timing closure (signal integrity)
- Flexible die size/shape
- High performance at high cost
DSP Processors

- Software programmable
- Single-cycle multiply-accumulate operations
- Real-time performance, simulation and emulation

Source: TI

Source: ADI
Programmable Logic Devices

Fuse-Based preprocessed die programmed (once only) in field
Prewired arrays with no need for dedicated manufacturing steps

PLA

Programmable OR Array

Programmable AND Array

Flexible to implement arbitrary functions in sum-of-product

PROM

Programmable OR Array

Fixed AND Array

Trade flexibility for density and performance, compared to PLA

PAL

Programmable AND Array

Fixed OR Array

Solid circles indicate fixed connection
Hollow circles indicates programmable connection

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Erasable PLD

Macrocell Altera Corp

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FPGAs

- Field programmable
- Fixed resources (metal-configured logic arrays, memories, PLLs, I/Os, DSP blocks, test circuitry)
- Designed for worse-case

Altera Stratix device architecture
Field Programmable Gate Arrays (FPGA)

- Repeatable Programming
- Ideal for prototyping
- Horizontal routing channel
- Switching Matrix for disjoint-cells and global interconnects
- Interconnect point
- Vertical routing channel
- Short Turn-Around Time
- Increasingly used in products

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Configurable Logic Blocks (CLB)

Combinational logic

Any function of up to 4 variables

Storage elements

R
Din
F
G
Clock
CE

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FPGA I/O Block
Embedded DSP Blocks

Implementation of a 180-Tap FIR Filter
Design Flows
ASIC Design: expense

• Definition, technology selection and planning
• RTL generation and synthesis, with verification
• Place, route, clock, test and power insertion, with verification
• Rule checking, data preparation, etc.
• Sample turn-around and testing
Device Selection Criteria

- Usable gates
- Memory structures
- High speed interfaces
- Performance and flexibility (relative to cell-based ASIC design)
- Availability of specialized IP: CPUs, DSPs, etc.
- Total price
- Turn-around time
- Easy design flow and tools
New Technologies Changing the ASIC Landscape

• Hardcopy FPGAs
  – HardCopy devices consist of a common set of base arrays implemented with the lower-level layers, and the top-level metal layers reserved for the customer’s design.
  – Reduce development costs and shorten time-to-market by eliminating ASICs’ long design cycles

• Structured ASICs
  – Base wafer defines logic cells, embedded functions and I/O
  – Customer design defines upper metal layers
  – Vendor provides clock, power, DFT routing
Altera Hardcopy Technology

- HardCopy provides considerable smaller size, performance and power consumption improvements over the FPGA counterparts
Altera Stratix GX Architecture