Second Tug of War Lab

Lab Date _____ **Lab Day _____**

Left Partner _____ **Right Partner _____**

Prelab **TA:_____** **Date _____** ☐

- Draw a simplified Hardware diagram for the divide by 128 counter.
  (You do not need to show the details of the combinational logic.)
- Draw a simplified Hardware diagram for the LFSR Random number generator.
  (You do not need to show the details of the combinational logic.)
- Write pseudo-code for the divide-by-128 counter.
- Write pseudo-code for the divide-by-128 testbench.
- Write pseudo-code for the LFSR.
- Write pseudo-code for the LFSR testbench.

Demo **TA: _____** **Date _____** ☐ ☐

- Exhibit/understand RTL and testbench code *left* *right*
- Proper RTL simulation of both LFSR and div-128
- (does not need to be self-checking)

Report **TA: _____** **Date _____** ☐

- Title Page, Intro
- Prelab
- All code/tb listings
- Commented waveforms for RTL AND Gate-level (add extra signals) Sims
- Cover Page
- Why didn't you finish in the lab?
- Screenshot of FPGA express with no problems on synthesized circuit.

Totals: **TA: _____** **Date: _____** ☐ ☐