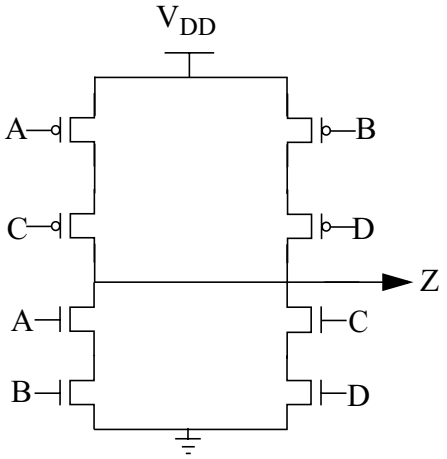
[1] (20 marks) Implement the following function in CMOS. Do not use over eight transistors in your implementation.

$Z = \overline{(AB) + (CD)}$

$\bar{Z} = (AB) + (CD)$ for NMOS network

$Z = (\bar{A} + \bar{B})(\bar{C} + \bar{D})$ for PMOS network



[2] (30 marks) True (T) or False (F)?

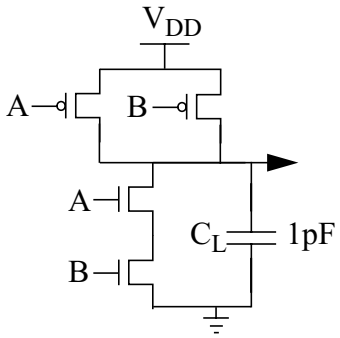
* F) Speed of CMOS circuits increase with increasing temperature.
* F) The lower the noise margins, the more reliable a circuit is.
* T) A transmission gate consists of a PMOS and a NMOS transistor in parallel.
* T) BJT digital circuits can be faster than CMOS.
* F) Switching threshold of a logic gate is the same as transistors' threshold voltage.
* T) A CMOS D-latch usually has a zero or negative hold time.
* T) PMOS transistors are slower than NMOS transistors with the same size.
* F) In an ideal logic gate, the output resistance is infinity.
* F) The body (substrate) of a PMOS transistor is usually connected to ground.
* F) Transistors in a digital CMOS circuit are always operating in the linear mode.

[3] (50 marks) Design a CMOS NAND gate with symmetric response to drive a bus capacitive load of 1 pF with a rising and falling propagation delay of 1 ns each. The supply voltage is 3 volts. Hint: realize that V_T of NMOS and PMOS transistors are not equal in the given technology.

Assumptions: a) transistors operate in saturation during transitions, b) ignore the diffusion capacitances and the internal capacitances of the NAND gate, c) channel-length modulation factor is zero, d) the input to the inverter is an ideal pulse, and e) do not use any magic equation or formula not discussed in your class. Find the following:

i) Dynamic Energy dissipation per cycle due to output (bus only).

ii) Static Energy dissipation per cycle.
iii) Sizes of all NMOS transistors.
iv) Sizes of all PMOS transistors.
v) Best-case rising and falling propagation delays.
vi) Sizes of all transistors in an equivalent NOR gate.



i) Dynamic Energy is given by

$$E_d = V^2_{DD} \cdot C_L = (3)^2 \cdot (1p) = 9pJ$$

ii) Static Energy, Es=0 because there is no static current.

iii) Falling delay $D_f = \frac{C_L \cdot V_{DD}}{2I_n}$ ---> $I_n = \frac{C_L \cdot V_{DD}}{2 \cdot D_f} = \frac{1p \cdot 3}{2 \cdot 1n} = 1.5mA$

According to assumption (a), use saturation formula:

$I_n = \frac{k'_n}{2}\frac{W_n}{L}(V_{GS} - V_{Tn})^2(1 + \lambda V_{DS})$ V_{GS}=V_{DD} and λ=0 (given in assumption c)

---> $W_n = \frac{2 \cdot L \cdot I_n}{k'_n \cdot (V_{DD} - V_{Tn})^2} = \frac{2 \cdot 0.5u \cdot 1.5mA}{40u \cdot (3 - 0.6)^2} = 6.5um$

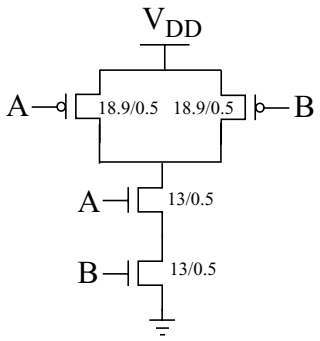
This is the size of NMOS transistor for an equivalent inverter. Hence, the effective width of NMOS network of NAND should be 6.5um. Which means each NMOS transistor in the NAND gate has width of $6.5 \times 2 = 13um$.

iv) For symmetric response D_r=D_f ---> Ip=In=1.5mA
similar to (iii), we have

$$W_p = \frac{2 \cdot L \cdot I_p}{k'_p \cdot (V_{DD} - V_{Tp})^2} = \frac{2 \cdot 0.5u \cdot 1.5mA}{15u \cdot (3 - 0.7)^2} = 18.9um$$

Again, this is width of PMOS transistor in an equivalent inverter. Hence, the effective worse-case condition width of PMOS network in the NAND gate should be 18.9um. Which means that both PMOS transistors have width of 18.9um.

W/L for all transistors are indicated in this figure



v) Best-case rising delay is when both PMOS transistors are conducting.
This gives twice the current and, hence half the delay.
Dr (best case)=1/2=0.5ns

vi) By looking at the sizing of the equivalent inverter,
we assign appropriate sizes for the transistor in NOR gate.

Notes:
1) Ideal of equivalent inverter was used here to design the NAND gate.
2) The diffusion and internal capacitances were ignored according to assumption (b). Even if the assumption was not given, we could still ignore those capacitances, because the output load capacitance is very large. The internal capacitances for submicron technologies are in the range of femto-Farads.
3)You can see that a NOR gate is much bulkier than a NAND gate with same performance.

Total width for $NOR = 37.5 \times 2 + 6.5 \times 2 = 88um$

Total width for $NAND = 18.9 \times 2 + 13 \times 2 = 63.8um$

This is why designers prefer to use CMOS NAND gates.