

Final Exam

Friday, April 27, Winter 2001

97.350: Digital Electronics

Department of Electronics, Carleton University

Instructor: Maitham Shams

Exam Duration: 3 hours

Booklet: None

Aids Allowed: Only Calculator

Last Name: _____
First name: _____
ID: _____

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Total
/20	/10	/15	/15	/15	/15	/10	/100

- * Write your name and ID number on all pages.
- * Attempt all questions. Making scheme for all questions are given.
- * If in a question you are asked to make an assumption, then you must use it.
- * Approximate thing is given for each question. If you follow that, you should have enough time at the end to review your answers.

Formula

$$I_{D(sat)} = \frac{k'_n W}{2L} (V_{Gs} - V_T)^2 (1 + \lambda V_{Ds})$$

$$I_{D(linear)} = k'_n \frac{W}{L} \left[(V_{DD} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

[1] Terminology (20 marks, 2 marks each, 30 minutes)

Briefly explain each of the following terms and point out its significance, i.e. why or where is it important? Write within the dedicated spaces.

a	HDL	Hardware Description Language is computer language for expressing the structure or behavior of hardware. It is used for two purposes: Simulation and synthesis of circuit (into FPGA or cell libraries)
b	Hazard	A condition in digital circuits which produces glitches. It results from unbalanced delays between propagation of a signal and its complement. Hazards are not important in synchronous circuits, but asynchronous circuits must be hazardous.
c	Clock Skew	Maximum difference in arrival time of clock signal between two points in a (synchronous) digital circuit. Circuits can tolerate some skew, but skew over some limit results in circuit malfunction, because some latches sample data and some not.
d	Scan Test	A method of testing (synchronous) sequential circuits, used to introduce test vectors inside circuit. Circuit under scan test has two modes: run and test. Flip flops are multiplexed to operate in either mode. Scan test makes testing different parts of a sequential circuit easy by setting them to 1 or 0.
e	Non-Blocking Assignment	A method of expressing an assignment in procedural Verilog. This allows flip-flops or latches in a procedure to use the old values obtained before executing the procedure. This also assures that the assignments run in parallel instead of sequences.
f	Noise Margin	A figure showing how noise tolerant a logic gate is. Two noise margins are defined: low and high. NML is the difference between maximum recognizable "0" input and nominal low output voltages. NMH is the difference between the nominal high output voltage and minimum recognizable "1" input.
g	Asynchronous Input Signal	Any input signal that its change is not synchronous with respect to test of circuit, and thus maybe unstable at clock edge. This represents all signal from outside world. To synchronize such inputs they go through flip-flops first.
h	Tri-state	A circuit similar to an inverter with an additional enable input. If enable is high, then it operates like a normal inverter, else (enable is low) there is no connection between output and V _{DD} or ground. This is called high impedance state. Tri-state buffers are used for sharing bus lines.
i	Procedural HDL coding	Coding the behavior of a circuit in HDL using "if", "case", and "while" statements like in C. This way is usually easier to code for the designer (no worries about deriving the logic) but harder on computer for synthesis (to translate behavior into logic gates).
j	Structural HDL Coding	Coding the components of a circuit as if all the logic gates used are known along with their connections. This is more difficult on designer (to work out logic), but easier for computer in synthesis (gates are known).

[2] Asynchronous Circuits and Testing (6+4=10 marks, 20 minutes).

*2.a] (6 marks) Describe the potential advantage of asynchronous circuits in speed, power and modularity?

--Speed of synchronous circuits is governed by its clock frequency, which has to be low enough so that clock period matches the worst case delay in the circuit. So synchronous circuits represent worst case delay. Some asynchronous circuits represent average case delay, because they can run as fast as data is processed (not bounded by clocks).

--Power dissipation: i) In synchronous circuits all latches and flipflops (or registers) operate and consume dynamic energy at each clock pulse, in spite of the fact that many of those registers may not have new data to store. There is no such waste of power in asynchronous circuits.

ii) Synchronous circuits also waste power on glitches due to hazard, while asynchronous circuits are designed to be hazard-free.

--Modularity: Asynchronous circuits are composed of functional module. with no regards to limiting issues inside each component. Only interfaces have to be well defined. This also leads to ii) between technology migration (incremental improvement). As asynchronous circuits can take advantage of new faster parts to improve speed. Synchronous circuits can not do that because the new parts also need to be operated with old frequency unless all parts changed.

*2.b] (4 marks) Describe the Stuck at fault models for testing and their advantage over complete tests.

Experience shows that most circuit faults are due to nodes sticking to Vdd or Gnd. There fore stuck-at 0 and stuck-at 1 fault models are made to detect them. This assumes that a fault is a “single” short circuit to Vdd or Gnd.

The advantage with respect to complete that is the lower number of test vectors needed. For N inputs, N+1 vectors are needed i.e, complexity of O(N). For complete test 2^N test vectors are needed.

[3] HDL code (9+6=15 marks, 25 minutes)

3.a] The following Verilog code is intended to synthesis a 1×2 de-multiplexer. The input is x, the output are y and z, and the switch is s. Assume that the “if-else” statement describes the behavior of the component correctly.

```
wire x, y;
reg z;
always @(x or y or z)
  begin
    if (!s) y=x;
    else z=x;
  end
```

i) (3 marks) Point out three wrong things in the above code.

1. y has to be defined as a register (reg y) because ti is output of procedure.
2. y and z must not be in the trigger list.
3. s must be in the trigger list.

ii) (4 marks) Does the code produce any latches? if “no” state why?

If “yes” state: a) how many latches are produced. b) The reason for each latch, and c) Is it possible to avoid having latches for this component?

--yes

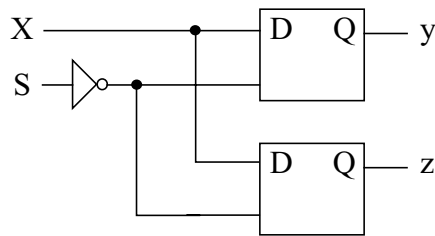
a--Two latches

b--One to store previous value of z, when s=0 (y=x)

One to store previous value of y, when s=0 (z=x)

c--No

*iii) (2 marks) Sketch a possible synthesized circuit for the proper code.



3.b] The following piece of Verilog code is intended to add two signed integers x and y. The result is z, which is intentionally mode one bit wider.

```
reg [3:0] x, y; reg [4:0] z;
assign x=-4'd3;
assign y=4'd5;
assign z=x+y;
```

*i) (3 marks) What is the numerical signed decimal result in z after running the code? What is the current result?

x=-3	+3=0011	--->	-3=1101	$\begin{array}{r} 1101 \\ + 0101 \\ \hline 10010 \end{array}$
y=5	+5=0101			

$z=10010=-01110=-14$

The current answer is $z=-3+5=+2$

This is because x and y need to be sign extended to fit z (5 bits)

ii) (3 marks) Replace the last “assign” statement with another single assign statement to fix the problem for any given signed x and y values.

$$z=\{x[3],x\}+\{y[3],y\}$$

[4] CMOS Delay and power (5+10=15 marks, 20 minutes)

4.a] (5 marks) A CMOS logic gate is operating on a supply of V driving a large capacitive load of C.

* i) What is the total energy dissipation per charging-discharging cycle?

$$E_T = CV_{DD}^2$$

*ii) What is the amount energy stored in C during charging?

$$E_s = \frac{1}{2}CV^2$$

*iii) If the above two values are different, explain why?

$$E_s = \frac{1}{2}E_T \quad \text{Other half is dissipated as heat by the PMOS network (pull-up network)}$$

*iv) What eventually happens to the energy stored in C during discharge?

Dissipates as heat by the pull down (NMOS) network.

(Don't go to grand, energy does not go to ground because $Gnd=0v$)

4.b] (10 marks) You have learned to techniques for calculating the delay of a CMOS logic gate, say an inverter. One technique uses the RC assumption and the other uses an average current formula. Show that the two techniques give almost similar results. *Assume no channel length modulation and assume that the transistors operate in saturation for high-to-low and low-to-high output transitions to $V_{DD}/2$.*

--The RC assumption $D=0.69RC$

--The average Current Formula:

$$D' = \frac{CV}{I} = \frac{CV_{DD}}{2I} \quad \text{where} \quad V = \frac{V_{DD}}{2}$$

$$I = \frac{k'W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DD}) = \frac{k'W}{2L}(V_{GS} - V_T)^2 \quad \text{since } \lambda = 0$$

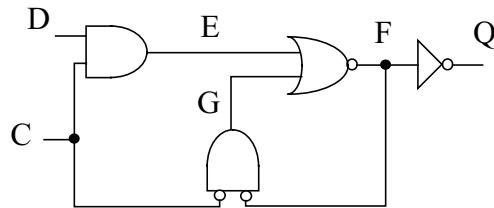
$$R = \frac{1}{2} \left(\left. \frac{V_{DS}}{I} \right|_{V_{DS} = V_{DD}} + \left. \frac{V_{DS}}{I} \right|_{V_{DS} = \frac{1}{2}V_{DD}} \right) \rightarrow R = \frac{1}{2} \left(\frac{V_{DD}}{I} + \frac{1}{2} \frac{V_{DD}}{I} \right) = \frac{3}{4} \frac{V_{DD}}{I}$$

$$\rightarrow D = 0.69 \left(\frac{3}{4} \frac{V_{DD}}{I} \right) C = 0.5175 \frac{V_{DD}}{I} C \cong 0.5 \frac{V_{DD}}{I} C = D'$$

This is true for falling and rising transitions

[5] Hazards (10+5=15 marks, 25 minutes)

The following circuit is a D-latch, with clock signal represented by C. It is alleged that this circuit is not worth fabrication because it produces glitches.



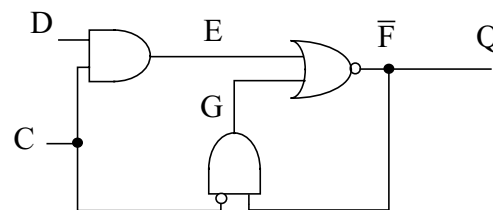
*5.a) (10 marks) Identify the type(s) and condition(s) for the hazard(s).

Redraw the circuit to remove the bubbles "0".

$$Q = E + G = DC + \tilde{Q}\bar{C}$$

$$\text{where } \tilde{Q} = \text{old } Q \text{ or } Q = D \cdot C + \bar{F} \cdot \bar{C}$$

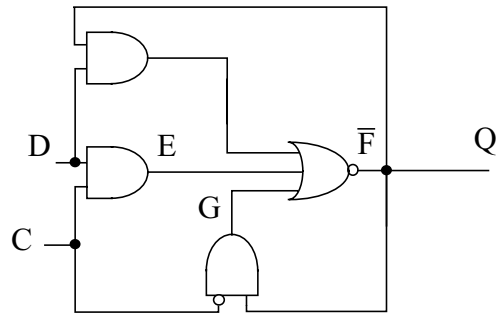
if $D=1$ and $\bar{F}=1$ ($F=0$),
then $Q=1C+1\bar{C}=1$ static 1 hazard.



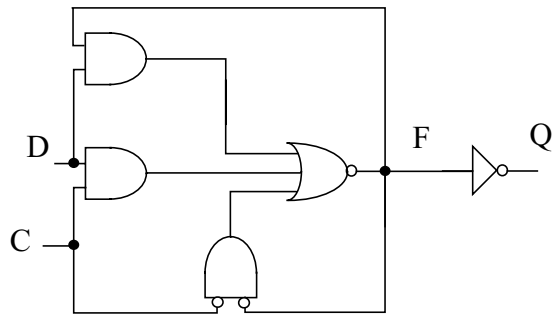
*5.b)

To mask the hazard, we must make sure Q stays high as C changes. Therefore the term to add is $D\tilde{Q}$ or $(D\bar{F})$

$$Q = DC + \bar{F}\bar{C} + D\bar{F} = DC + \tilde{Q}\bar{C} + D\tilde{Q}$$



OR



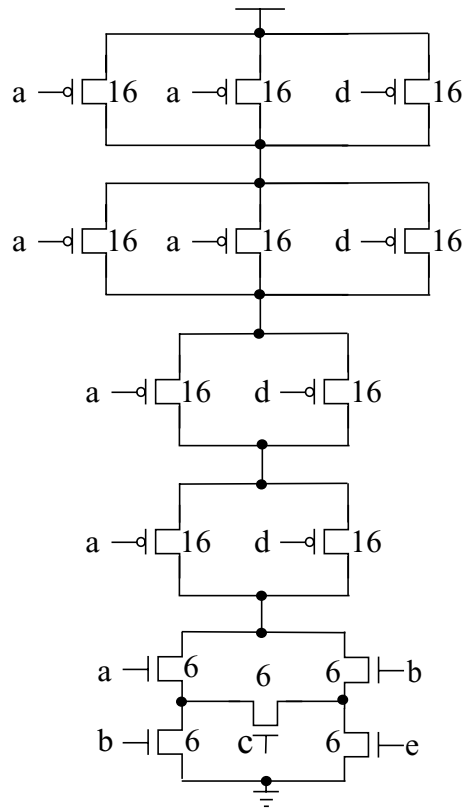
[6] CMOS implementation (15 marks, 5 marks each, 20 minutes)

In the following figure the NMOS network of a complex CMOS logic gate is shown.

*6.a) Express the Boolean function of the gate.

*6.b) Draw the corresponding CMOS network inside the square.

*6.c) Size the transistors such that, in worst case, the logic gate has the same output resistance as an inverter with PMOS $W/L=4$ and NMOS $W/L=2$.



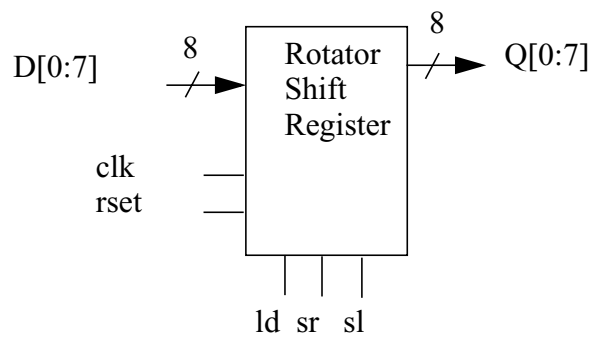
$$\bar{F} = ad + be + ace + bcd$$

$$F = \overline{ad + be + ace + bcd} = (\bar{a}\bar{d})(\bar{b}\bar{e})(\bar{a}\bar{c}\bar{e})(\bar{b}\bar{c}\bar{d}) = (\bar{a} + \bar{d})(\bar{b} + \bar{e})(\bar{a} + \bar{c} + \bar{e})(\bar{b} + \bar{c} + \bar{d})$$

Sizes are shown on figure.

[7] HDL Design (10 marks, 20 minutes)

Write the full Verilog code for an eight bit shift register (i.e the carry out is fed back). It has an asynchronous Reset (rset), Clock (clk), Load (ld, for loading the register with data in a parallel fashion), shift left (sl), and shift right (sr) signals. You must use the given names in the figure.




```

module shiftreg (Q, D, ld, sr, sl, rset, clk)
  input [7:0] D;
  input ld, sr, sl, rset, clk;
  output [7:0] Q;
  reg [7:0] Q;
  wire [7:0] D;
  wire ld, sr, sl, rset, clk;
  always @(posedge clk or posedge rset)
    begin
      if (rset) Q<==0;
      else if (ld) Q<==D;
      else if (sr)
        begin
          Q<==Q>>1;
          Q[7]<==Q[0];
        end
      else if (sl)
        begin
          Q<==Q<<1;
          Q[0]<==Q[7];
        end
    end
end

```