Department of Electronics Student Name _____

ELEC3500 Digital Design

Mid-Term Examination Student Number _____

October 23, 2012 10:05 AM –11:25 AM R. Mason

answer all questions on the exam sheet provided, one 8.5 x 11 crib sheet allowed

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1. (5 points) multiple choice, circle the **BEST** answer.

(a) A three input NOR gate with input values of "1", "X" and "Z" would have an output value of ?

i) "Z"
ii) "0"
iii) "1"
iv) "X"

(b) Verilog code of the form **always @(school)** could synthesize to:

i) a latch
ii) a flip-flop
iii) a class
iv) a clock

(c) What is the typical hold time of a CMOS flip-flop:

i) -0.5nS
ii) 0.5nS
iii) 1uS
iv) -1uS

(d) Which transistors changes will decrease the output delay of a CMOS inverter:

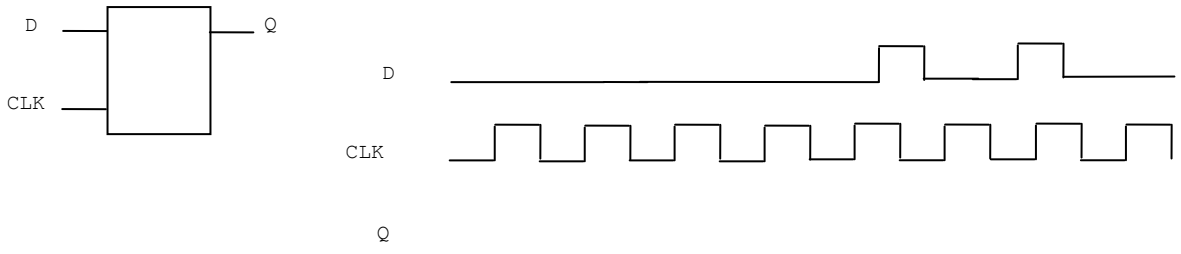
i) increase $|V_T|$, increase W
ii) increase $|V_T|$, decrease W
iii) decrease $|V_T|$, increase W
iv) decrease $|V_T|$, decrease W

(e) A case statement should have a default case to:

i) make all cases mutually exclusive
ii) to prevent a synchronous reset
iii) to prevent unwanted latches
iv) make a stronger case

2. (10 points) Answer the following:

(a) Draw the expected output waveform for Q in the following circuit with the given signals for D and CLK (assume setup and hold times are 0).



(b) Draw a gate level (i.e. AND, OR, etc.) schematic for the hardware that would be produced from the following Verilog behavioral code? Is there anything wrong with this code?

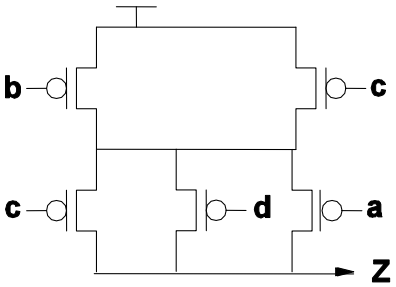
```
module midterm(a, b, c);
input [3:0] a;
input  b;
output [7:0] c;
register [7:0] c;
always @ (a)
begin
  c = 0;
  if (b) begin
    case (a)
      4'b0000 : c = 8'h01;
      4'b0001 : c = 8'h02;
      4'b0010 : c = 8'h04;
      4'b0011 : c = 8'h08;
      4'b0100 : c = 8'h10;
      4'b0101 : c = 8'h20;
      4'b0110 : c = 8'h40;
    endcase
  end
end
endmodule
```

(c) A CMOS inverter has V_{OH}=0.8V, V_{OL}=0.1V, V_{IH}=0.6V, V_{IL}=0.4V. Calculate the noise margins for this circuit. What would happen to the output if the input to this circuit was at 0.5V?

NM_L =_____ V If input = 0.5V , output = _____

NM_H =_____ V

(d) Complete the complex CMOS gate below by adding the require NMOS transistors. Write the logic equation for the completed circuit (i.e. Z = ?)



(e) Write a COMPLETE (including module statement etc.) verilog module using BEHAVIOURAL code to implement an 10-to-1 multiplexer (i.e. 10 input, 1 output and 4 select lines)

3. (5 points) A 2.0V supply voltage, FIVE input CMOS NAND gate has transistors with the following characteristics: W_P= 2um, W_N= 2um, L=0.2um, k_p'= 50uA/V^2, k_n'= 100uA/V^2, V_T=0.5V, λ=0. Where k_p' and $k_n'$are the process gains and W_P and W_N are the transistor widths for PMOS and NMOS transistors respectively. If the gate has an output load capacitance of 0.1pF and assuming all transistors are in saturation mode, calculate (a) worst case rising delay, (b) worst case falling delay, (c) resize the NMOS transistor widths (keeping all NMOS transistors with the same width) so that the worst case falling delay is equal to the worst case rising delay (d) calculate the dynamic power dissipation when the output is toggling at 100 MHz.

(a) _____ ns

(b) _____ ns

(c) _____ um

(d) _____ uW

$$I_d = \frac{1}{2}k'\frac{W}{L}(V_{gs}-V_t)^2(1-\lambda V_{ds}) \qquad D = \frac{CV_{dd}}{2I} \qquad P = CV_{dd}{}^2 f$$