Department of Electronics Student Name _____

ELEC3500 Digital Design

Mid-Term Examination Student Number _____

October 27, 2010 4:05 PM – 5:25 PM R. Mason

answer all questions on the exam sheet provided, one 8.5 x 11 crib sheet allowed

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1. (5 points) multiple choice, circle the **BEST** answer.

(a) A two input NAND gate with input values of "0" and "X" would have an output value of ?
   i) "1"
   ii) "0"
   iii) "X"
   iv) "Z"

(b) Verilog code of the form **always @(posedge c)** could synthesize to:
   i) a latch
   ii) a flip-flop
   iii) a pulse
   iv) a clock

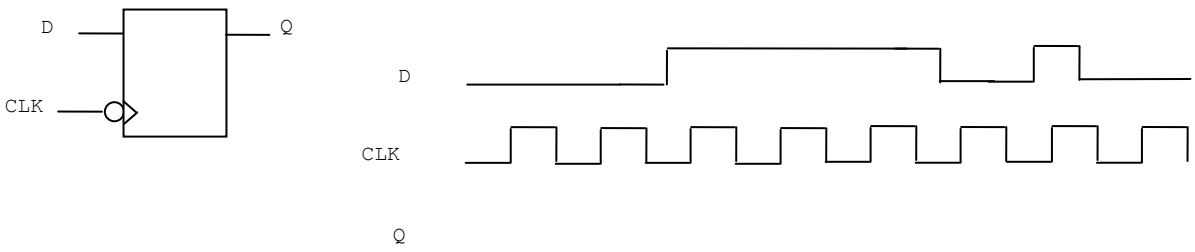
(c) Which of the following is true for a NMOS transistor?
   i) turned on when input is logic 0
   ii) good at pulling output to logic 0
   iii) current decreases as gate voltage increases
   iv) negative threshold voltage

(d) What is the typical output delay for a CMOS Inverter?
   i) 100 ps
   ii) 100 ns
   iii) 100 us
   iv) 100 ms

(e) A verilog test bench has:
   i) no timing statements
   ii) most of the synthesizable blocks
   iii) all chip input signals
   iv) all of the structural verilog code

2. (10 points) Answer the following:

(a) Draw the expected output waveform for Q in the following circuit with the given signals for D and CLK (assume setup and hold times are 0).

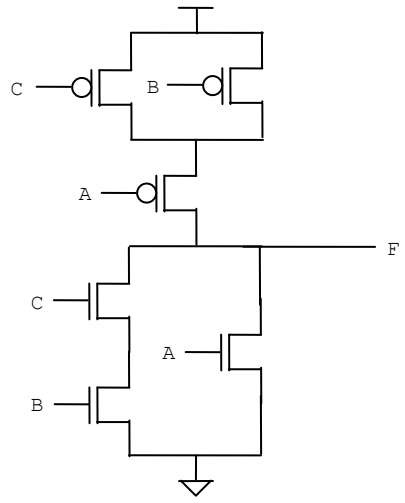


(b) What does the following verilog code do? Is there anything wrong with this code?

```
input clk, rset;
output count, TC;
wire [3:0] count, TC;
always @(posedge clk or posedge rset)
begin
        if (rset) count = 0;
        else count <= count+1;
        TC  <= & count;
end
```

(c) Why does a CMOS gate pull its output all the way to VDD (i.e. the supply voltage) for V_{OH}? Draw a CMOS inverter circuit to help explain this operation.

(d) Write the logic equation for the following circuit (i.e F = ?). What is the logic value of the output F when the A and B inputs are logic "0" and the C input is logic "1"?



(e) Draw a transistor level (i.e. **TRANSISTORS ONLY**, no gate symbols) circuit diagram showing a static CMOS latch using only inverters and transmission gates. The circuit should have two inputs (D and CLK) and one output (Q). The circuit should have 10 transistors (i.e. three inverters and two transmission gates). The latch should be in transparent mode (i.e. D input passes directly to Q output) when the CLK input in logic "1".

3. (5 points) A 1.8V supply voltage, THREE input CMOS NOR gate has transistors with the following characteristics: W= 2um, L=0.2um, $k_p' = 20uA/V^2$, $k_n' = 60uA/V^2$, $V_T=0.5V$, $\lambda=0$. Where k_p' and k_n' are the process gains for PMOS and NMOS transistors respectively. If the gate has an output load capacitance of 0.1pF and assuming all transistors are in saturation mode, estimate (a) worst case rising delay, (b) worst case falling delay, (c) best case rising delay, (d) best case falling delay, (e) dynamic power dissipation when the output is toggling at 10 MHz.

(a) _____ ns

(b) _____ ns

(c) _____ ns

(d) _____ ns

(e) _____ uW

$$I_d = \frac{1}{2}k'\frac{W}{L}(V_{gs}-V_t)^2(1-\lambda V_{ds}) \qquad D = \frac{CV_{dd}}{2I} \qquad P = CV_{dd}{}^2 f$$