Midterm Exam, Winter 2004, February 26

97.350: Digital Electronics

Department of Electronics, Carleton University

Instructor: Maitham Shams **Name:** _____

Aids: Closed Book **ID:** _____

Q1	Q2	Q3	Total
/20	/30	/50	/100

Write your name and ID number on all pages. There are three questions. Read the instructions here and for each question carefully to avoid regrets!

- You have *one hour* to write the exam. No questions answered *at all*.
- If you are asked to make an assumption, then you **must** use it, but only for that particular question. State and justify any additional assumptions you make in a question.
- After marking, exam papers are copied in random before returning to students. Students who want their papers to be remarked, **must** hand in the papers to the instructor by the end of the class or lab section in which they get their marked papers back.

Formula

$$
\begin{aligned}
C_{ox} &= \frac{\varepsilon_{ox}}{t_{ox}} \\
C_j &= \frac{C_{j0}}{(1 - V_D/\phi_0)^m} \\
K_{eq} &= \frac{-\phi_0^m}{(V_H - V_L)(1-m)}[(\phi_0 - V_H)^{1-m} - (\phi_0 - V_L)^{1-m}] \\
V_T &= V_{T0} + \gamma(\sqrt{|\,-2\phi_F + V_{SB}\,|} - \sqrt{|\,-2\phi_F\,|}) \\
I_D(\text{sat}) &= \frac{k'}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \\
I_D(\text{linear}) &= k'\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)
\end{aligned}
$$

Data

NMOS: $L = 0.5\ \mu$m, V_{TO}=0.6 V, $k' = 40 \times 10^{-6}$ A/V^2, λ=0 V^{-1}, C_j=0.5 fF/μm^2, C_{jsw}=0.3 fF/μm, t_{ox}=150E-10 m.

PMOS: $L = 0.5\ \mu$m, V_{TO}=-0.7 V, $k' = 15 \times 10^{-6}$ A/V^2, λ=0 V^{-1}, C_j=0.5 fF/μm^2, C_{jsw}=0.3 fF/μm, t_{ox}=150E-10 m.

General: m=0.5 (abrupt junction), ϕ_0=0.6 V, ε_{ox}=3.5 E-13 F/cm.

[1] (20 marks) Implement the following function in CMOS. Do not use over *eight* transistors in your implementation.

$$Z = \overline{(AB) + (CD)}$$

[1] (30 marks) Circle True (T) or false (F)?

- (T / F) Speed of CMOS circuits increase with increasing temperature.
- (T / F) The lower the noise margins, the more reliable a circuit is.
- (T / F) A transmission gate consists of a PMOS and an NMOS transistor in parallel.
- (T / F) BJT digital circuits can be faster than CMOS.
- (T / F) Switching threshold of a logic gate is the same as transistors' threshold voltage.
- (T / F) A CMOS D-latch usually has a zero or negative hold time.
- (T / F) PMOS transistors are slower than NMOS transistors with the same size.
- (T / F) In an ideal logic gate, the output resistance is infinity.
- (T / F) The body (substrate) of a PMOS transistor is usually connected to ground.
- (T / F) Transistors in a digital CMOS circuit are always operating in the linear mode.

[3] (50 marks) Design a CMOS NAND gate with symmetric response to drive a bus capacitive load of 1 pF with a rising and falling propagation delay of 1 ns each. The supply voltage is 3 volts. *Hint:* realize that V_T of NMOS and PMOS transistors are not equal in the given technology. *Assumptions:* a) transistors operate in saturation during transitions, b) ignore the diffusion capacitances and the internal capacitances of the NAND gate, c) channel-length modulation factor is zero, d) the input to the inverter is an ideal pulse, and e) do not use any magic equation or formula not discussed in your class. Find the following:

i)Dynamic Energy dissipation per cycle due to output (bus only).

ii)Static Energy dissipation per cycle.

iii)Sizes of all NMOS transistors.

iv)Sizes of all PMOS transistors.

v)Best-case rising and falling propagation delays.

vi)Sizes of all transistors in an equivalent NOR gate.