# Lab 3 : CMOS Sequential Logic Gates

## Design and Specification of Sequential Logic Gates and Library Cell

Digital circuits are made of gates. Up to now you used gates as boxes. You assumed they give out 0 or 1 and their delay is always constant. Gates are made of transistors. Transistor gates do not always give out "1"= 5V. Without proper precautions it may be less than 3V. The gate propagation delay is not constant. It depends strongly on output loads and input loads. In a two input gate it will be different for each input.

In this lab you will build gates from transistors, and observe how the properties of the transistors makes the gates less than ideal. You will design the gates that make up a flip-flop and finally a flip-flop. The sequence of circuits you will build are:r

a) The transmission gate, an electronic switch.
b) The MUX, both analog and digital.
c) The latch built from a MUX
d) The master-slave D flip-flop, made from latches.

# 1. Transistors as Pass Switches

MOS transistors can also be used as pass switches for digital or analog signals. They are used to switch audio signals around inside stereo systems.

### The NMOS Pass Switch

There are some limitations on these switches. Redraws FIGURE 2.1a as FIGURE 2.9b. Then remembers from Section 0.3 that the source can never rise above $V_G$-$V_{TH.}$

You should be able to deduce that near the peak of the waveform the output will be clipped.

*Q1. Using simulations sketch the output for FIGURE 2.1. Explain your results..*

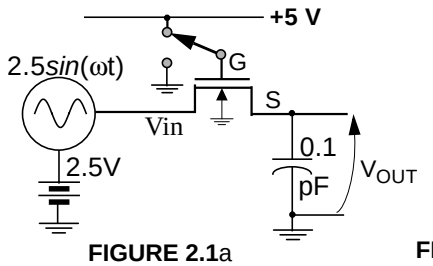


**FIGURE 2.1**a

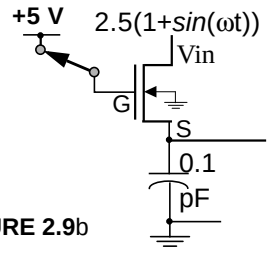


**FIGURE 2.9**b

### The PMOS Pass Switch

The PMOS pass switch is harder to understand than the NMOS one. Think of the capacitor holding a charge and acting as the $V_{DD}$ of the circuit. The distortion will come when Vin is low.

*Q2. Using simulations sketch the output for FIGURE 2.2. Explain your results.*

**FIGURE 2.2**a

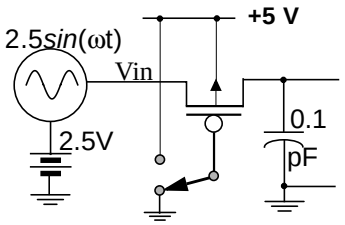
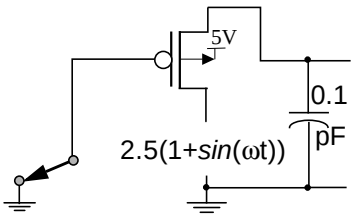



**FIGURE 2.10**b

PMOS switch redrawn




### The CMOS Transmission Gate

The transmission gate contains two transistors. One conducts well for the signals for which the other conducts poorly.

*Q3. Sketch the output for FIGURE 2.3 as seen from your simulation.*

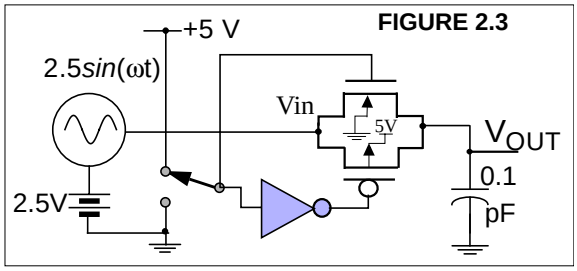



**FIGURE 2.3**

*Q4. Explain the results as compared to the previous two cases*

# 2. The Mux

The MUX switches an output between two inputs as dictated by a control signal. Here:

**if(ctrl= =1) y=d; else y=q;**

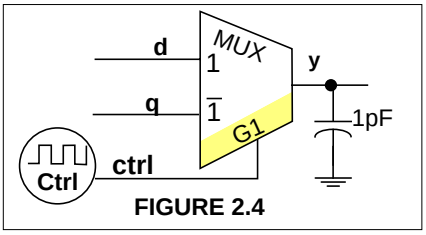



**FIGURE 2.4**

### Transmission-Gate MUX.

Build a MUX out of two of the transmission gates and an inverter. You will need to put voltmeters at ***ctrl*** and ***y***.

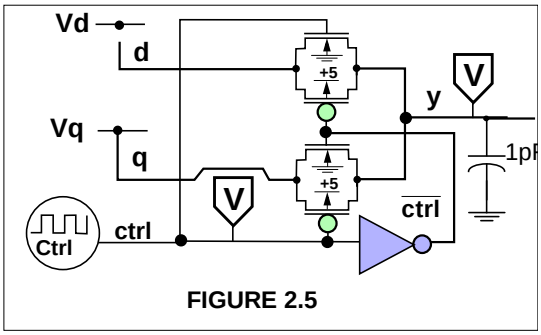



**FIGURE 2.5**

### Signal Inputs

Connect a square wave generators to ***ctrl***. Connect some voltage Vd, (maybe 4.5V) at d, and another for Vq, (maybe 0.5V) at q This allows ***y*** to be seen to change when the MUX switches from ***q*** to ***d***.

*Q5. Sketch the circuit and output.*

**Testing the MUX**

Determine the propagation delay between the time the ***ctrl*** rises and the switched output appears at ***y***. This is called $t_{CHYV}$ (time from Control High to Y Valid). Most of these propagation delays are measured between 50% points.

Make the ***ctrl*** rise and fall times fast enough (under 1ns). Otherwise you will be reporting that $t_{CHYV}$ is proportional to the input rise/fall time. The Spice pulse generator can be set from its attributes as shown in FIGURE 2.6.

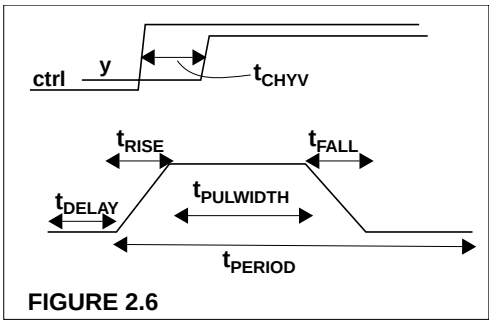


FIGURE 2.6

*Q6. Record $t_{CHYV}$ and the similar signal $t_{CLYV}$ (Control Low Y Valid).*

# 3. The D-latch

Convert the MUX to a D-Latch. FIGURE 2.15b will work for a MUX constructed of gates but not transmission gates. The conservation of energy has everything to do with this. A gate has gain.

FIGURE 2.7 MUX made from gates

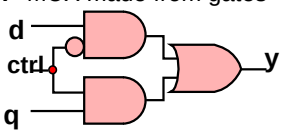
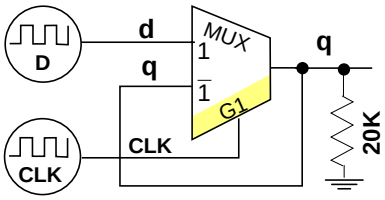


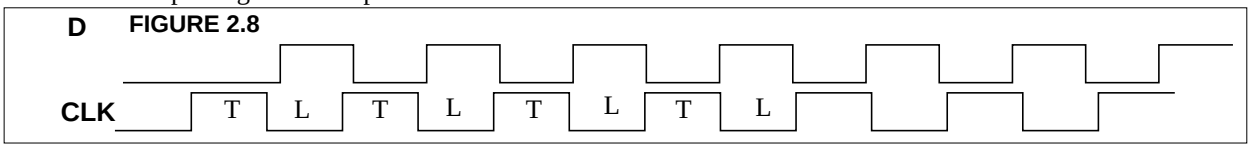

FIGURE 2.15b D latch from a MUX




*Q7. Add components to your D latch work to make it work with transmission gates.*[1]

In order to check the setup time of the latch one must change ***d*** and ***clk*** at the same time. Use two square-wave generators, CLK has a period about 0.25 ns faster than D but with [(1/2 period) + 2ns] larger initial delay (TDELAY). This will allow the ***d*** and ***clk*** input edges to slide past each other.

FIGURE 2.8




**Testing The Latch**

Make sure your latch functions as a transparent latch. If the output decays with time, you are just looking at the storage on a charged capacitor. This is not a static latch! It will forget if the clock is slow. The 10K load resistor was used to be sure the output decay would be fast enough to see easily

*Q8. Sketch your circuit and the part of your test waveform that proves the latch functions as a transparent latch.*

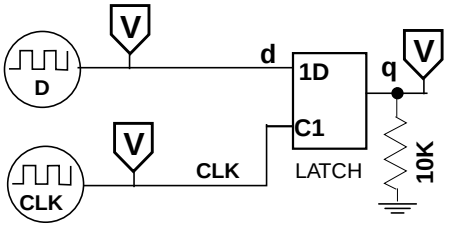


FIGURE 2.9

1. The demonstration Pspice is limited to 10 transistors. You will have to use the inverter made without transistors or use the full Pspice simulator.

### The Setup Time

If the ***d*** input changes too close to the CLK edge the ***d*** input will not be captured as ***q***. However if the ***d*** input is stable at least a ***setup time*** before the CLK edge, the at stable value will be captured.

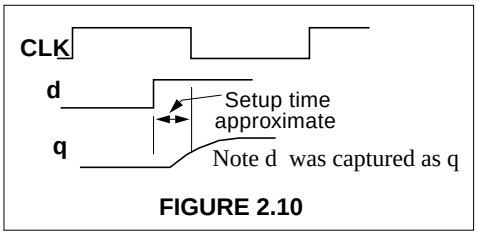


FIGURE 2.10

*Q9. Measure the setup time using your sliding waveforms. You may want to extend the time of the simulation. The length is controlled by the attributes in the* ***oscilloscope*** *or the.TRAN command in SPICE.*

The symbol for a transmission gate is ⊗ or ⋈
Your latch should be as shown in FIGURE 2.11 or FIGURE 2.12.

Add a 2pf capacitive load to ***q*** and see if that effects the setup time.

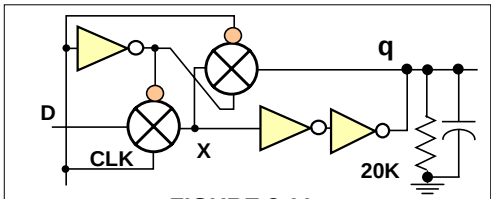


FIGURE 2.11

*Q10. Measure the new setup time. Comment on why an output load would change the setup time which would appear to be associated only with the input.*

*Commercial latches add an extra inverter as a buffer amplifier to keep the load from influencing the setup time.*

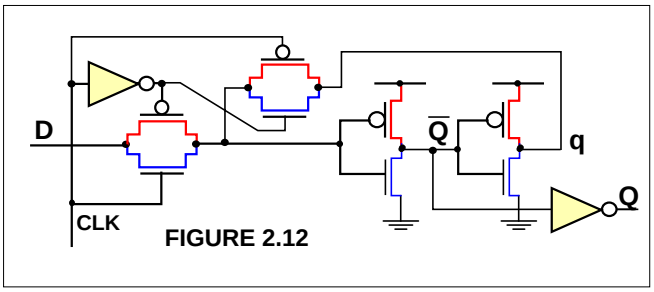


FIGURE 2.12

### The Hold Time

The hold time is the length of time the ***d*** signal must be stable after the clock changes to be sure of capturing the correct value. Good latches have zero or even a negative hold time. The same sliding waveforms used to measure the setup time can also measure the hold time.

*Q11. Measure the hold time.*

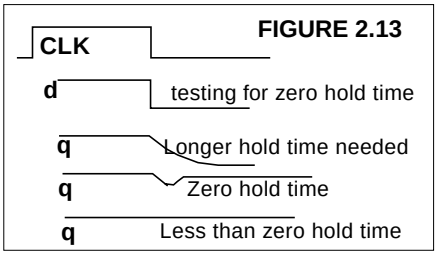


FIGURE 2.13

# 4. The D Flip-Flop

The master-slave D flip-flop is made by connecting two D latches in series. The two are transparent on opposite clock edges.

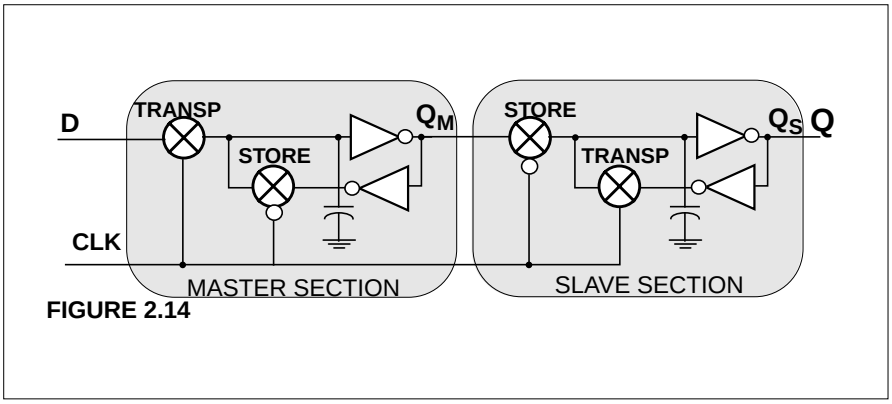
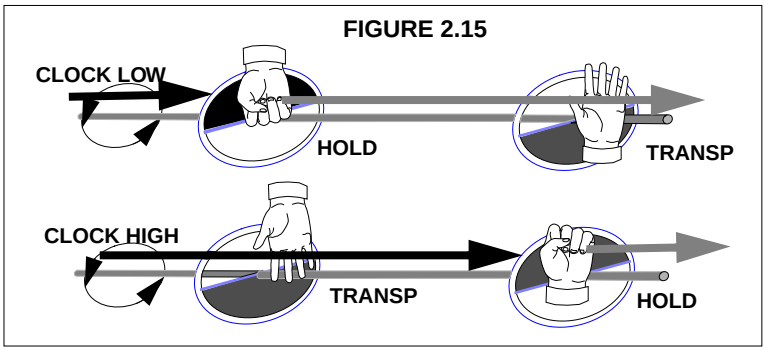


FIGURE 2.14




When the master is high it holds the output and the transparent slave lets it through. When the master goes transparent, the slave holds the previous output so it does not change.

**Design**

Design a D flip-flop and implement a model in Spice. Use the model to determine the following specifications:
(i) the setup time, (ii) the hold time, (iii) the clock to output time $t_{CHQV}$, (iv) the high output voltage with a 0.5 mA output current (The output high and loaded with a 10K resistor), and (v) the low output voltage when sinking 0.5 mA. ( The output low and loaded with a 10K resistor connected to $V_{DD}$.)

# 5. Deliverables:

- Fill out a cover sheet.
- Demo your work to a TA.
- Answer all questions.