Lab 2 : CMOS Combinational Logic Gate

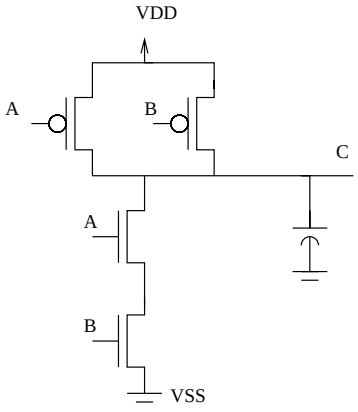
Design of the CMOS Combinational Logic Gates

CMOS inverters and combinational logic gates are made of PMOS and NMOS. In this lab, you will do the schematic capture and simulate the CMOS combinational logic gates. By sizing the transistors in the combinational logic gates, you can manipulate the performances of the logic gates.

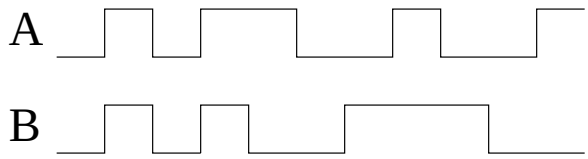
In this section, we implment NOR and NAND gates. Sizing the transistors in these combinational CMOS logic gates, we get the same delay charateristics as the CMOS inverter in previous lab. Assume a capacitive load of C_L = 1 pF at the output of all gates for simulations.

1. NAND Gate

Design a two-input NAND gate, as shown below:



Determine the size of the transistors to achieve the same performance as a CMOS inverter with PMOS W/L = 40/5 and NMOS W/L = 20/5. Simulate the circuit using the given waveforms below. (use the piecewise linear waveform in SPICE)



Q1. What are the sizes of the NMOS and PMOS transistors?

Q2. Plot the input and output waveforms and make sure the gate functions properly for all input cases. Measure the delay in each of the four cases. Present the data in the table.

Q3. Which input combination defines the worst-case delay?

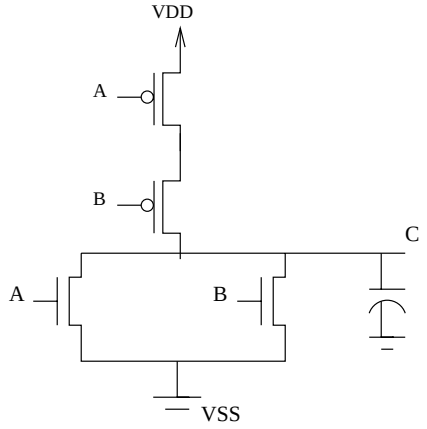
Q4. Which input combination defines the best-case delay?

Q5. What is the relation between the numerical rising delay values of the two cases in Q3 and Q4? Can you explain why?

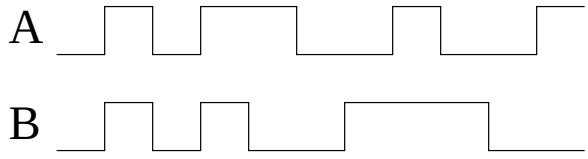
Q6. Which input combination defines the falling delay?

2. NOR Gate

Design a two-input NOR gate, as shown below:Design a two-input NOR gate



Determine the size of the transistor to achieve the same performance as the CMOS inverter in the previous section. Simulate the circuit using the given waveforms below.



Q7. What are the sizes of the NMOS and PMOS transistors?

Q8. Plot the input and output waveforms and make sure the gate functions properly for all input cases. Measure the delay in each of the four cases. Present the data in the table.

Q9. Which input combination defines the worst-case falling delay?

Q10. Which input combination defines the best-case falling delay?

Q11. What is the relation between the numerical falling delay values of the two cases in Q9 and Q10? Can you explain why?

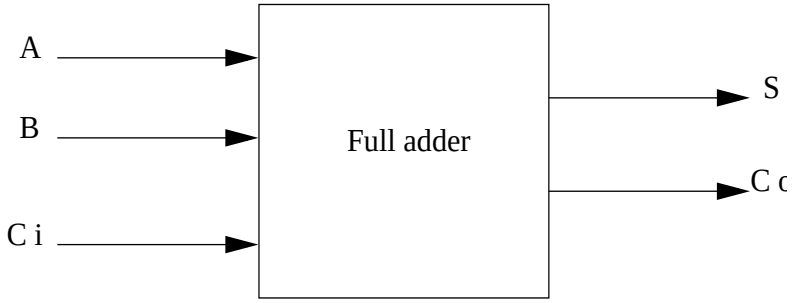
Q12. Which input combination defines the rising delay?

Q13. How is the total size of the designed NOR gate compared to the NAND gate with the same performation? This is why designers usually prefer to use CMOS NAND gates rather than CMOS NOR gates.

3. Full adder circuit

Implement the carry-out (C_o) of a full-adder circuit in conventional CMOS using 12 transistors only. The inputs are A, B, and C_i. Prove that the circuit works for all eight combinations using simulations.

(**Hint:** The expression for carry-out is: $C_o = AB + AC_i + BC_i$. It is more efficient to implement $\overline{C}_o$ and invert it to get C_o).



4. Deliverables:

- Fill out a cover sheet.
- Demo your work to a TA.
- Answer all questions.