# Lab 1 : MOSFET Devices & CMOS Inverter

## 1. Design and Specification of MOSFET Devices

Digital circuits are comprised of million of transistors. Transistors are made of MOSFET, the metal-oxide semiconductor field-effect transistor. This is a particular kind of FET, field-effect transistor. MOSFET is extremely popular in the industry. Compared to BJTs or other devices, MOSET transistors are small and can be well packed together on the high density chip. MOSFET manufacturing process is relatively simple. Digital logic and functional block can be implemented with MOSFETS exclusively. (no resistors or capacitors are needed)

In this lab, you will do the schematic capture and simulate the MOSFET as a switch. The enhancement-type MOSFETs are used. Observe how the properties of the MOSFET makes the switch less than ideal.

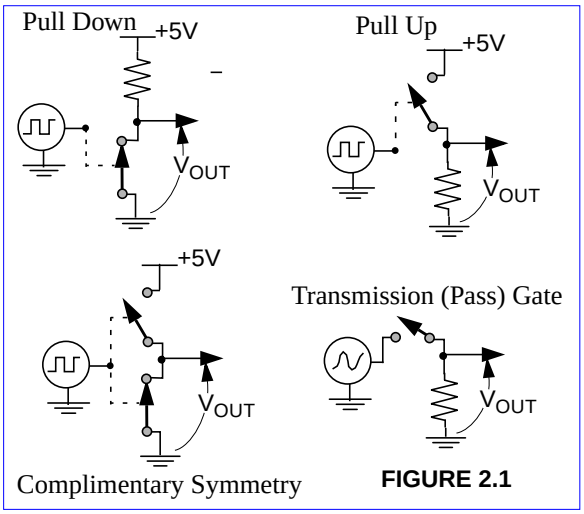


FIGURE 2.1

### 1.1 Transistors as Switches

Digital gates are made from switches. FIGURE 2.1 shows four types of switch connections. We will look at how to use MOS transistors in each type of connection.

a) PMOS and NMOS as pull down switches.
b) PMOS and NMOS as pull up switches.
c) Placing PMOS and NMOS in complimentary symmetry (CMOS) gates.
d) The transmission gate, or pass gate.

### 1.2 NMOS transistors.

#### 1.2.1 Transistor Pulling Down

To use transistors in digital circuits one must know how to connect them to get the full 0V to 5V output swing

Here, with the gate at 5V, the transistor is on (conducting), so one would expect $V_{OUT}$ to be close enough to 0V to be a useful digital signal. (Unless a poor designer made R too low, say 100 Ω.)

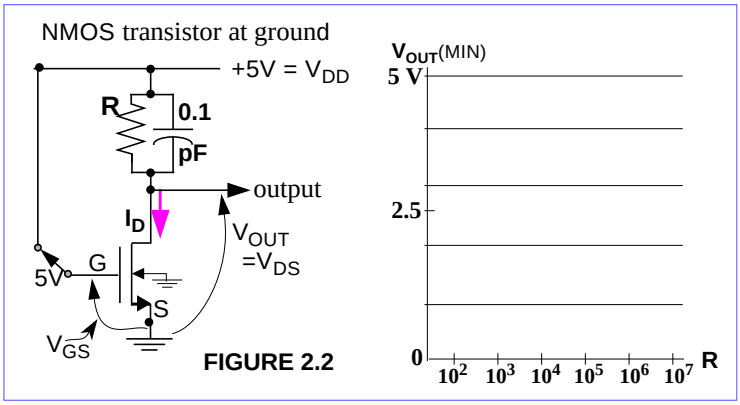


FIGURE 2.2

*Q1. Use SPICE to find the range of R over which the circuit of FIGURE 2.2 can deliver a digitally useful low $V_{OUT}$, say less than 0.5 V. Plot the graph Vout min versus R.*

The 0.1pF capacitor is stray circuit capacitance. Many MOS circuits have only stray capacitance (no resistors) in them, particularly if they feed only other MOS circuits.

*Q2. Using simulations plot $\sqrt{I_d}$ versus $V_{GS}$ and from that find the threshold voltage of the NMOS transistor.*

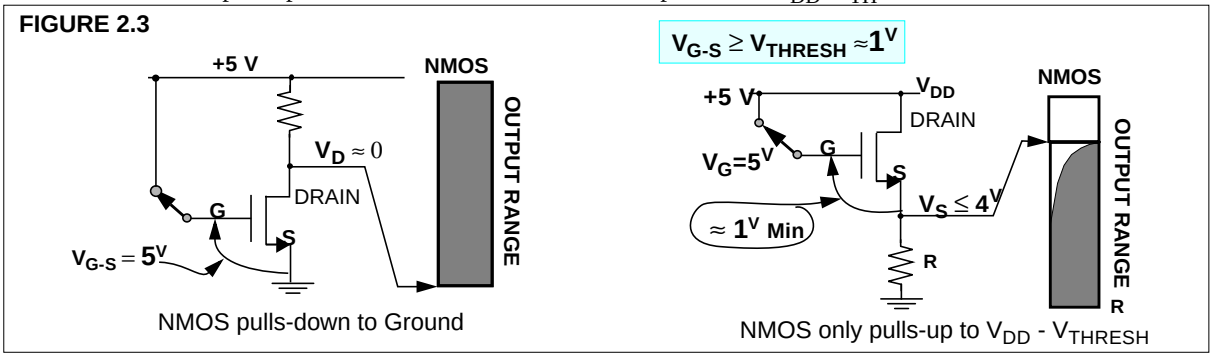
## 1.2.2 Transistor at Top End ($V_{DD}$End) Of Circuit.

Now consider the transistor connected at the top of instead of the bottom (FIGURE 2.4). With the gate at 5V, the transistor is turned on, so one would expect $V_{OUT}$ to be close to 5V. But is it really that close?

### The Threshold Voltage

The MOS transistors used in gates have a minimum $V_{GS}$ to turn on called $V_{TH}$ (threshold voltage). Typically $V_{TH}$ is 0.5 to 1.5V. Even at $V_{GS} = V_{TH}$ conduction is poor. One needs a voltage many times higher to give a low channel resistance. FIGURE 2.3 shows how even with $V_G$=5V, $V_{GS}$ can be much smaller. Further the pull-up connection can never have an output above $V_{DD}$-$V_{TH}$.

**FIGURE 2.3**




*Q3. Use SPICE to find $V_{OUT}$ for a range of R. Especially find out how close the output can get to 5V. Plot the graph Vout max versus R.*

*You should find the output (Source) can never rise closer than $V_{THRESHOLD}$ to the gate, and then only when R is megohms.*

*Q4. Comment: Would you think digital circuits would perform better when NMOS transistors were connected to pull the output up or down?*

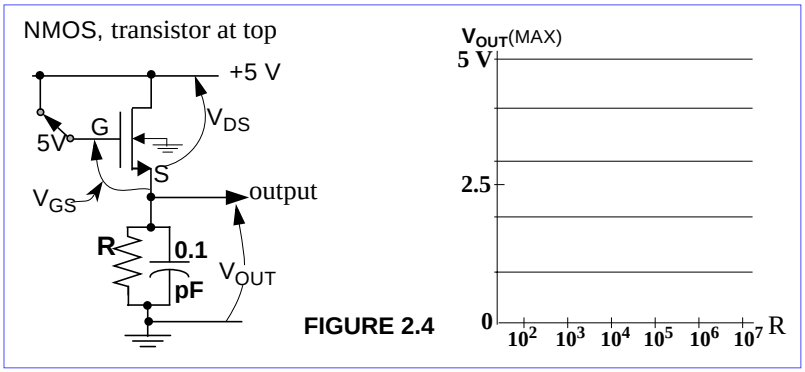



**FIGURE 2.4**

*Q5. Plot $I_d$ for NMOS transistor widths ranging from 20μm to 100μm in 10μm intervals. Justify your observation intuitively. (Keep the length at 5μm)*

*Q6. Plot $I_d$ for NMOS transistor lengths ranging from 5μm to 30μm at 5μm intervals. Justify your observation. (Keep the width at 30μm)*

# 1.3 PMOS transistors

## 1.3.1 Transistor At Ground End

*Q7. Use SPICE to find $V_{OUT}$ for a range of R. Plot the graph Vout min versus R. How close can $V_{OUT}$ get to 0V?*

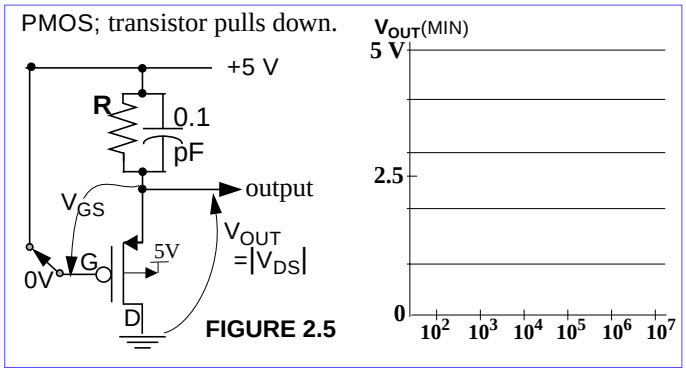


FIGURE 2.5

## 1.3.2 Transistor Pulling Up

*Q8. Use SPICE to plot $V_{OUT}$ max vs R, particularly find the maximum $V_{OUT}$.*

*Q9. Using simulations plot $\sqrt{Id}$ versus $V_{GS}$ and from that find the threshold voltage of the PMOS transistor.*

*Q10. Comment: Would you think digital circuits would perform better when PMOS transistors were connected to pull the output up or down?*

*Q11. Plot $I_d$ for PMOS transistor width 20µm to 100µm at 10µm intervals. How does PMOS current level compare to NMOS ones? Why?.*

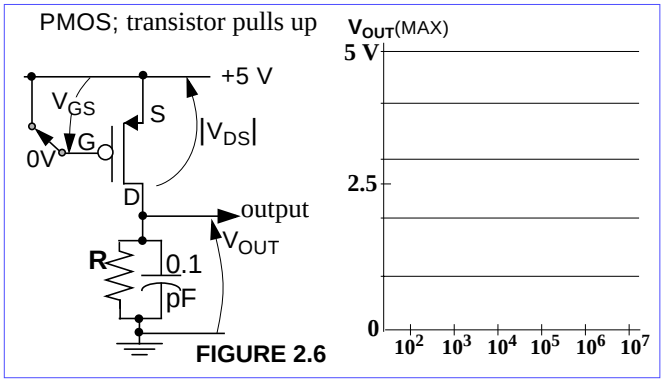


FIGURE 2.6

# 2. Design of the CMOS Inverter

CMOS inverters are made of PMOS and NMOS. PMOS and NMOS are complementary with each other. PMOS transistor is conducted with logic zero applied to the its gate terminal. Otherwise, PMOS is off. The performance of NMOS is complementary with that of PMOS. Also, the sizes and position of transistor have big impacts on its performances.

In this part of the lab, you will do the schematic capture and simulate the CMOS inverters.

# 2.1 CMOS Inverter

There were two problems with making logic gates with a transistor and a resistor:
i) Getting a full 0-5V output swing. This was solved by choosing correctly between NMOS and PMOS.
ii) When the transistor was off there was a long slow RC time constant while the capacitor discharged through the resistor.

In CMOS logic gates two transistors are used and no resistors. One transistor pulls the output up and another to pulls it down. There is no large time constant.

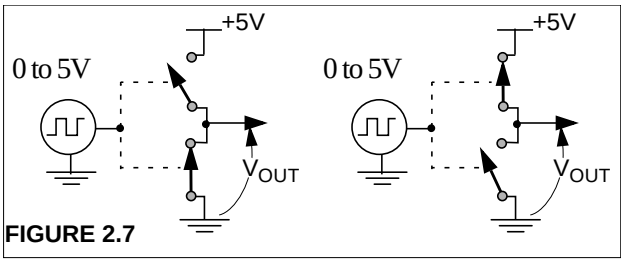


FIGURE 2.7

*Q12. Classify the inverter circuits of FIGURE 2.8 as "won't work," "will work with poor output swing," and "will work well". Explain which one does not have the inverting structure.*

*Q13. Using simulations sketch the output waveform from circuits (A) and (B). Use the knowledge you gained from Section 1.3 to explain.*

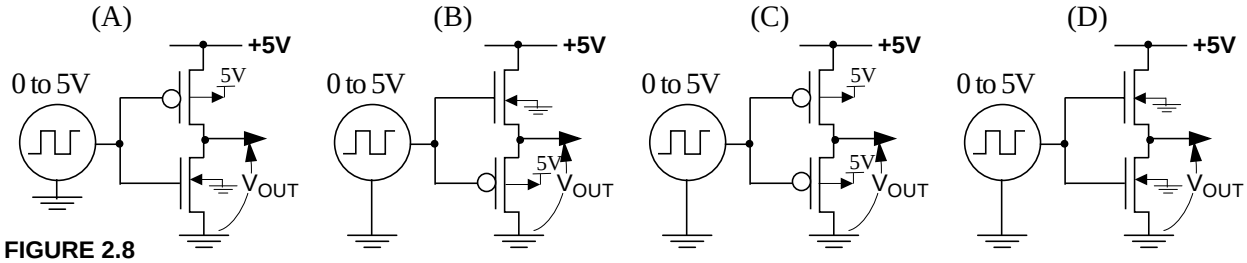


FIGURE 2.8

*Q14. Add a 0.5 pF capacitor to the output of the CMOS inverter and measure the falling and rising times (10% - 90% swing), and measure the falling and rising delays (50% input swing to 50% output swing).*

*Q15. Which delay is larger? Why? (Hint: look into PMOS and NMOS transistors relative sizes.)*

*Q16. For what size ratio you expect a symmetric output (i.e. almost equal rising and falling times, and almost equal rising and falling delays.) Prove your suggestion by simulation results. You may want to try a number of cases such that the rising and falling delays differ by less than 1%.*

*Q17. Now set the width of PMOS to 40 microns and the width of NMOS to 20 microns. Plot VTC of the inverter by sweeping the input from 0V to 5V at 0.2V intervals and measuring the output. On the graph show and measure the Switching Threshold, the input and output high and low voltage levels, and the high and low noise margins.*

*Q18. Try Q17 with the width values used in Q16. What difference do you realize? Explain.*

**Width/Length**

An important factor when building MOS transistors is W/L. Just as a long thin wire has more resistance than a short thick one, a transistor with a small W/L has more resistance than one with a large W/L.

In this lab the default size for transistors is W=30u, L=5u. (u or μ means micron $=10^{-6}$ of a meter. Visible light is 0.4 to 0.7μ.) In 1998 a minimum W of 0.5μ (wavelength of green light) is common. Next year it will be 0.35. A large W is used for transistors that need to deliver power like bus drivers.

**Substrate Bias**

In MOS transistors, the substrate is always made a reversed biased diode with the channel. In PMOS this means connecting the substrate to VDD. In NMOS it is connected to ground. In SPICE it will be necessary to use the 4-terminal transistors for transmission gates The substrate in the 3-terminal ones are connected to the source, which is correct only for conventional gates.

# Deliverables:

- Fill out a cover sheet
- Demo your work to a TA
- Answer all questions