CARLETON UNIVERSITY

FINAL
EXAMINATION
April 2011

Duration: 3 Hours **No. of Students: 108**

Department Name & Course Number: ELEC 3500 Digital Electronics

Course Instructor(s): Ralph Mason

AUTHORIZED MEMORANDA
Calculator and one 8.5" x 11" Crib Sheet Only

Students **MUST** count the number of pages in this examination question paper **before** beginning to write, and report any discrepancy to a proctor. This question paper has **12** pages.

This examination question paper **MAY NOT** be taken from the examination room.

In addition to this question paper, students require: an examination booklet **No**
a Scantron sheet **No**

Last Name: _____

First Name: _____

ID: _____

Q1	Q2	Q3	Q4	Q5	Total
/20	/20	/20	/20	/20	/100

- Write your name and ID number clearly on front page
- Attempt all questions. Marking scheme for all questions are given
- If in a question you are asked to make an assumption, then you must use it
- Answer all questions on the pages provided

1. Terminology (20 Marks, 2 marks each)

Briefly explain each of the follow terms and point out its significance, i.e. why or where is it important? Write within the dedicated spaces

A	Verilog “initial” Procedure	
B	Verilog "assign" statement	
C	Verilog blocking assignment	
D	Verilog test bench	
E	t_{CHQV}	
F	Gray code	
G	Clock divider	
H	Asynchronous signal	
I	$(\bar{a} + a)(a)$	
J	Static 0 Hazard	

2. Verilog Code (20 Marks)

2a) (10 marks) The following verilog code has inputs I and S and output Q.

```
module exam(band, clk, rst);
input clk;
output band;
reg [7:0] bcount;
wire band;
  always @(posedge clk or negedge rst)
    begin
        if (rst==0) bcount<=3'b100;
      else
        bcount = {bcount[6:0], bcount[7]^bcount[6]};
    end
  assign band = bcount[5]&(~bcount[6]);
endmodule
```

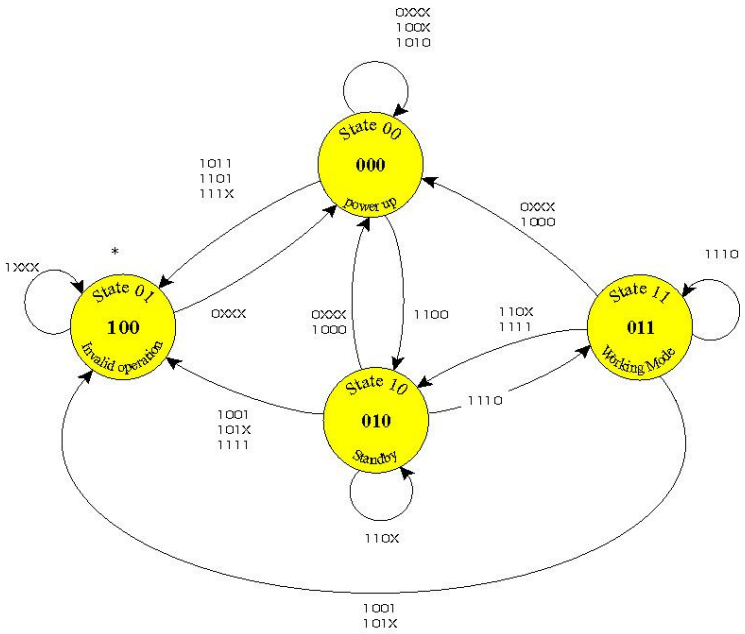
i) (2 marks) What is the intended function of the verilog code?

ii) (2 marks) Point out any bad things with the above code

iii) (3 marks) Does the code produce any latches? Why?

iv) (3 marks) Sketch a possible synthesized circuit for the code.

2b) (10 marks) Write complete verilog code (i.e complete module) for the following state diagram. Inputs for the module are x[3:0], clk and reset. Inputs x and reset are synchronous with clk. Transistions between states are controlled by the x input as shown on the state diagram. The states are State 00, 11, 10 and 01 which have state assignments of 000, 011, 010 and 100 respectively. The reset state is State 00.



3. Hazards (20 Marks)

i) (14 marks) Identify and mask any hazards in the following expression. Also, show that no new hazards are created.

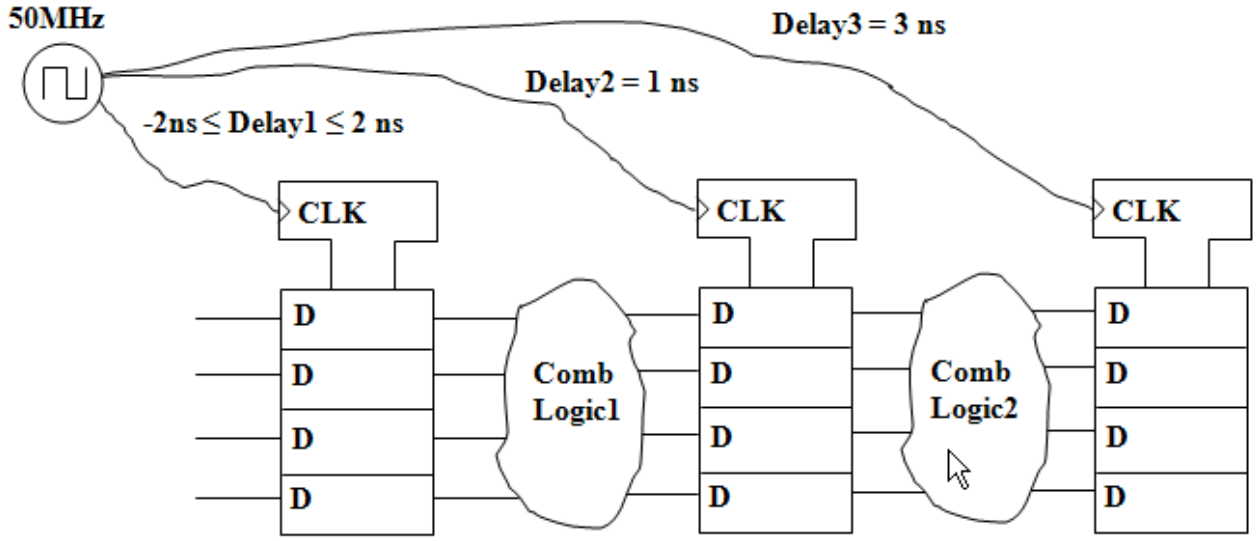
$F = (gc\,\bar{a} + aeb)\,(c\,\bar{g} + d\,\bar{c}\,b)$

ii) (3 marks) Explain and show in a logic expression why a sum of products circuit representation should not have any dynamic hazards?

iii) (3 marks) Give the logic function $f = (\bar{a} + b)(c + a)$. Draw the Karnaugh map for this function and identify any hazards on the Karnaugh map.

4. Timing (20 Marks)

4a) For the following synchronous circuit the registers have T_{setup} = 2 ns, T_{hold} = -1 ns and T_{CHQV} = 1 ns.

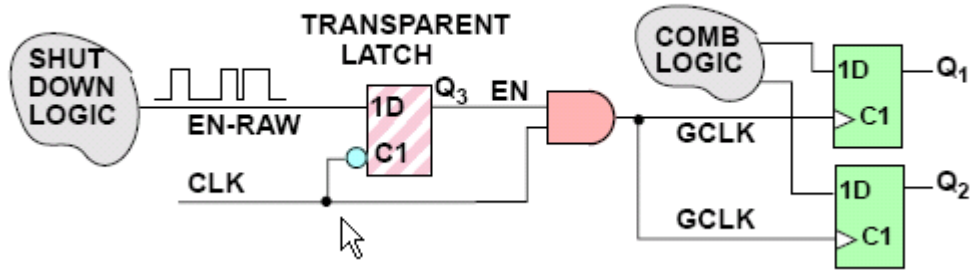


i) (8 marks) Determined the minimum and maximum propagation delays for combinational logic block 1 (Comb Logic1) and combinational logic block 2 (Comb Logic2). Show how you calculate this.

ii) (4 marks) If both combinational blocks have a minimum delay of 5 ns and a maximum delay of 7ns how large could Delay2 become and the circuit still operate correctly? Show how you calculate this.

iii) (3 marks)) If both combinational blocks have a minimum delay of 4 ns and a maximum delay of 5 ns how large could the clock frequency become and the circuit still operate correctly? Show how you calculate this.

4b) The following circuit can be used to provide clock gating.

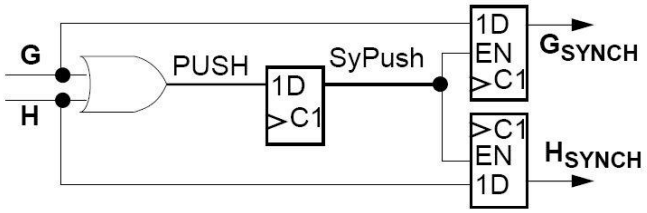


(i) (3 marks) Draw a timing diagram for the circuit and explain why there are no false clock edges.

(ii) (2 marks) Is this still true if there is clock skew? Why?

5. Asynchronous Circuits (20 Marks)

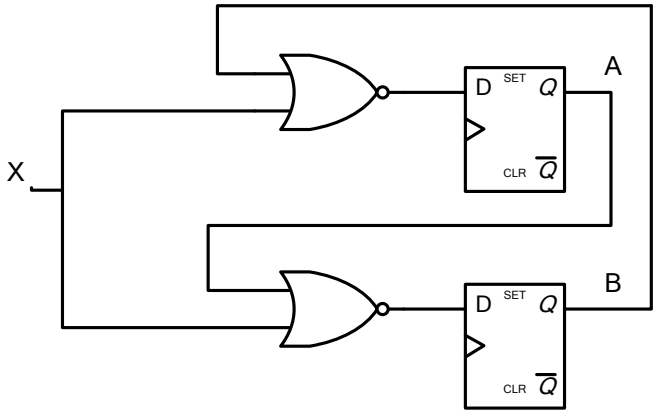
5a) For the tug of war circuit below



i) (5 marks) Using a timing diagram, explain how the SyPush signal is used as a handshaking signal to interface the asynchronous push button latch to the rest of the circuitry

ii) If a much faster clock was available (e.g. 10 MHz) and you only had to decide who won the round within one clock period, how could you simplify the tug of war circuitry? Draw a timing diagram to show new operation. Explain any disadvantages with your new circuit.

5b) (i) (5 marks) What is wrong with the following synchronous state machine that has asynchronous input X



(ii) (5 marks) Show how you would fix it without adding or removing any flip-flops? Show your work.