Final Exam
Winter 2008
ELEC 3500: Digital Electronics
Department of Electronics

Instructor:	Ralph Mason	Exam Duration:	3 hours
Booklets:	None	Number of Pages:	12
Aids Allows:	Only Calculator	Number of Students:	70

Last Name: _____

First Name: _____

ID: _____

Q1	Q2	Q3	Q4	Q5	Q6	Total
/20	/20	/20	/20	/10	/10	/100

- Write your name and ID number clearly on front page
- Attempt all questions. Marking scheme for all questions are given
- If in a question you are asked to make an assumption, then you must use it
- Answer all questions on the pages provided

1. Terminology (20 Marks, 2 marks each)

Briefly explain each of the follow terms and point out its significance, i.e. why or where is it important? Write within the dedicated spaces

A	Verilog "Always" Procedure	
B	Verilog synchronous Reset	
C	Verilog blocking assignment	
D	Synthesis	
E	Verilog Trigger List	
F	Positive Clock Skew	
G	Clock Gating	
H	Single Variable Change Hazards	
I	Non Maskable Hazards	
J	Dynamic Hazard	

2. Verilog Code (20 Marks)

2a) (10 marks) The following verilog code has inputs I and S and ouput Q.

```
module block(Q, I, S);
input [3:0] I;
input [1:0] S;
output Q;
always @(S)
begin
        case (S)
                2'b00: Q = I[0];
                2'b01: Q = I[1];
                2'b10: Q = I[2];
                2'b11: Q = I[3];
        endcase
end
endmodule
```

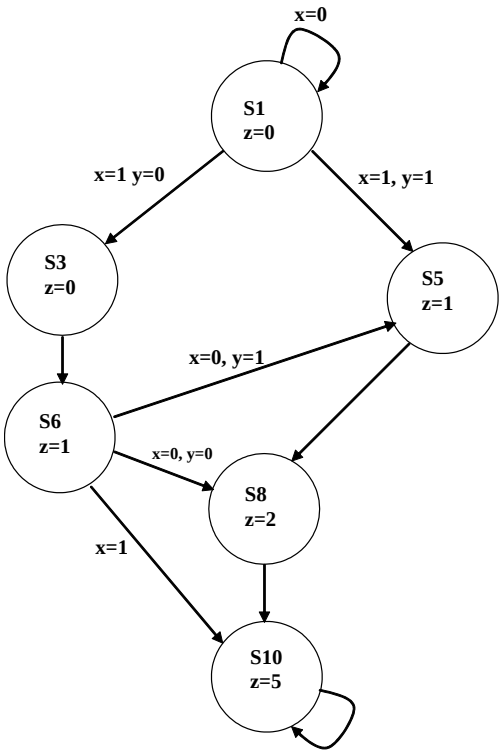
i) (2 marks) What is the intended function of the verilog code?

ii) (2 marks) Point out any bad things with the above code

iii) (3 marks) Does the code produce any latches? Why?

iv) (3 marks) Sketch a possible synthesized circuit for the code.

2b) (10 marks) Write complete verilog code (i.e complete module) for the following state diagram. Inputs for the module should be x, y, clk and reset, output is z and states are S1,S3,S5,S6,S8,S10.



3. Hazards (20 Marks)

i) (14 marks) Identify and mask any hazards in the following expression. Also, show that no new hazards are created.

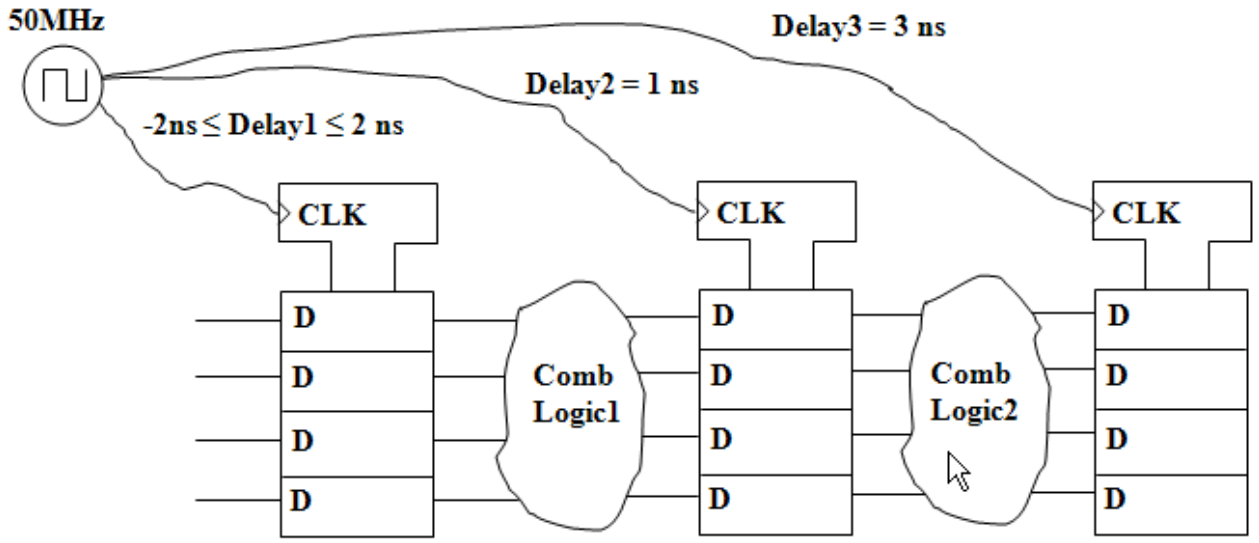
$F = (ce\,\bar{a} + a\,b)\,(c\,\bar{b} + d)$

ii) (3 marks) Explain and show in a logic expression why a products of sums circuit representation should not have any static 1 hazards?

iii) (3 marks) Draw a 4 variable Karnaugh map and show a single variable and a two variable change hazard.

4. Timing (20 Marks)

4a) For the following synchronous circuit the registers have T_{setup} = 1 ns, T_{hold} = 0 and T_{chqv} = 1 ns.

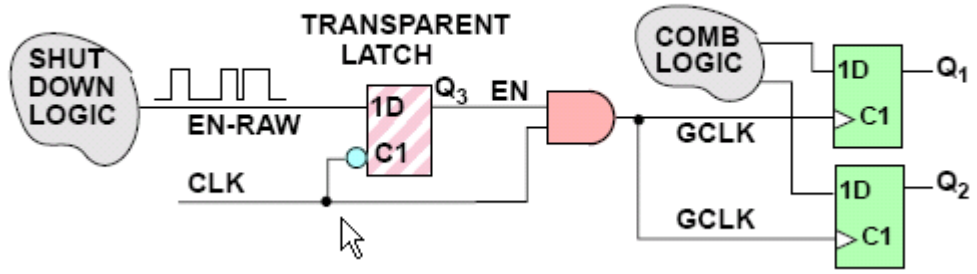


i) (8 marks) Determined the minimum and maximum propagation delays for combinational logic block 1 (Comb Logic1) and combinational logic block 2 (Comb Logic2). Show how you calculate this.

ii) (4 marks) If both combinational blocks have a minimum delay of 4 ns and a maximum delay of 6ns how large could delay2 become and the circuit still operate correctly? Show how you calculate this.

iii) (3 marks)) If both combinational blocks have a minimum delay of 3 ns and a maximum delay of 4 ns how large could the clock frequency become and the circuit still operate correctly? Show how you calculate this.

4b) The following circuit can be used to provide clock gating.

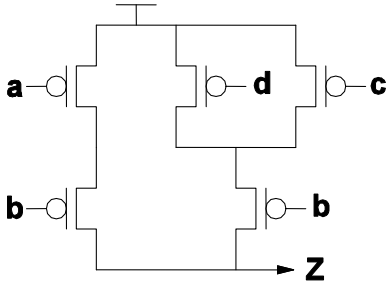


(i) (3 marks) Draw a timing diagram for the circuit and explain why there are no false clock edges.

(ii) (2 marks) Is this still true if there is clock skew? Why?

5. CMOS Implementation (10 Marks)

Consider the following CMOS logic gate where all transistors have a channel length of 1um.



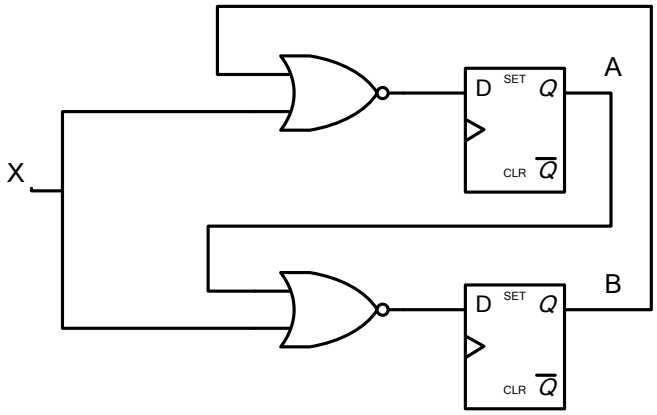
i) (3 marks) Draw and label the NMOS transistor gates to complete the implementation.

ii) (3 marks) Find the output (Z) boolean expression in terms of the primary inputs.

iii) (4 marks) Size the transistors such that the circuits worst case rise times and fall times are equivalent in performance to an inverter with PMOS W/L of 3 and NMOS W/L of 1 (show your work).

6. Asynchronous Circuit (10 Marks)

(i) (5 marks) What is wrong with the following synchronous state machine that has asynchronous input X



(ii) (5 marks) Show how you would fix it without adding or removing any flip-flops? Show your work.