Final Exam

Friday, 27 April, Winter 2001

97.350: Digital Electronics

Department of Electronics, Carleton University

Instructor:	Maitham Shams	**Exam Duration:**	3 hours
Booklets:	None	**Number of Pages:**	10
Aids Allowed:	Only Calculator	**Number of Students:**	120

Last Name: _____

First Name: _____

ID: _____

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Total
/20	/10	/15	/15	/15	/15	/10	/100

- Write your name and ID number clearly on all pages.
- Attempt all questions. Marking scheme for all questions are given.
- If in a question you are asked to make an assumption, then you must use it.
- Approximate timing is given for each question. If you follow that, you should have enough time at the end to review your answers.

Formula

$$I_D(\text{sat}) = \frac{k'_n}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$$I_D(\text{linear}) = k'_n\frac{W}{L}\left((V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right)$$

[1] Terminology (20 marks, 2 marks each, 30 minutes)

Briefly *explain* each of the following terms and point out its *significance*, i.e. why or where is it important?. Write within the dedicated spaces.

a	HDL	
b	Hazard	
c	Clock Skew	
d	Scan Test	
e	Non-Blocking Assignment	
f	Noise Margin	
g	Asynchronous Input Signal	
h	Tri-State Buffer	
i	Procedural HDL coding	
j	Structural HDL Coding	

[2] Asynchronous Circuits and Testing (6+4=10 marks, 20 minutes).

- **2.a]** (6 marks) Describe the potential advantage of asynchronous circuits in *speed*, *power*, and *modularity*?

- **2.b]** (4 marks) Describe the Stuck-at fault models for testing and their *advantage* over complete tests.

[3] HDL Code (9+6=15 marks, 25 minutes)

3.a] The following Verilog code is intended to synthesis a 1×2 de-multiplexer. The input is x, the outputs are y and z, and the switch is s. Assume that the "if-else" statement describes the behaviour of the component correctly.

```
wire x, y;
reg z;
always @(x or y or z)
   begin
      if (!s) y=x;
      else z=x;
   end
```

- i) (3 marks) Point out three wrong things in the above code.

- ii) (4 marks) Does the code produce any latches? If "no" state why?
  If "yes" state: a) how many latches are produced, b) The reason for each latch, and c) Is it possible to avoid having latches for this component?

- iii) (2 marks) Sketch a possible synthesized circuit for the code.

3.b] The following piece of Verliog code is intended to add two *signed* integers x and y. The result is z, which is intentionally made one bit wider.

```
reg [3:0] x, y; reg [4:0] z;
assign x=-4'd3;
assign y=4'd5;
assign z=x+y;
```

- i) (3 marks) what is the numerical signed decimal result in z after running the code? What is the correct result?

- ii) (3 marks) Replace the last "assign" statement with another *single* assign statement to fix the problem for any given signed x and y values.

[4] CMOS Delay and power (5+10=15 marks, 20 minutes)

4.a] (5 marks) A CMOS logic gate is operating on a supply of V driving a large capacitive load of C.

- i) What is the total energy dissipation per charging-discharging cycle?

- ii) What is the amount of energy stored in C during charging?

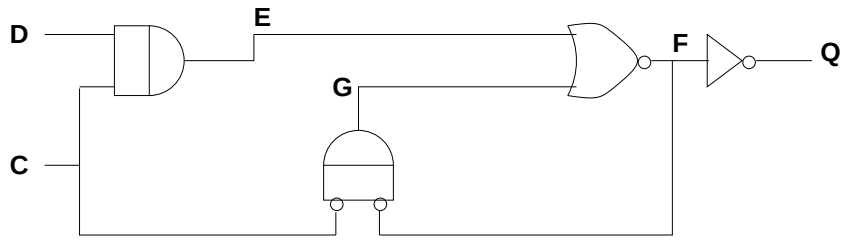
- iii) If the above two values are different, explain why?

- iv) What eventually happens to the energy stored in C during discharge?

4.b] (10 marks) You have learned two techniques for calculating the delay of a CMOS logic gate, say an inverter. One technique uses the RC assumption and the other uses an average current formula. Show that the two techniques give almost similar results. *Assume no channel length modulation and assume that the transistors operate in saturation for high-to-low and low-to-high output transitions to* $V_{DD}/2$.

[5] Hazards (10+5=15 marks, 25 minutes)

The following circuit is a D-latch, with the clock signal represented by C. It is alleged that this circuit is not worth fabrication because it produces glitches.



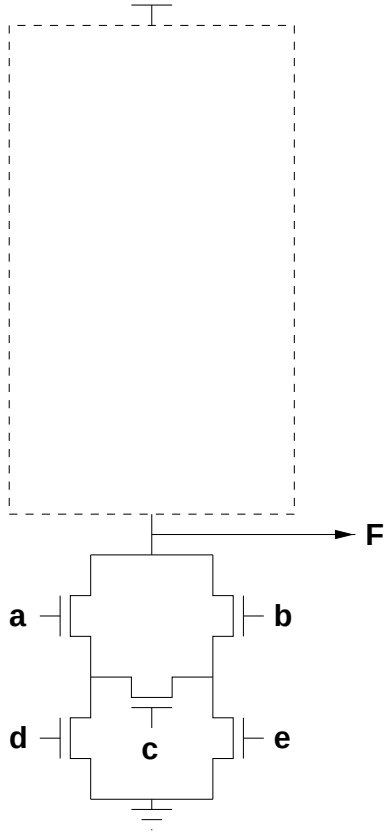
- **5.a)** (10 marks) Identify the type(s) and condition(s) for the hazard(s).

- **5.b)** (5 marks) Mask the hazard(s).

[6] CMOS Implementation (15 marks, 5 marks each, 20 minutes)

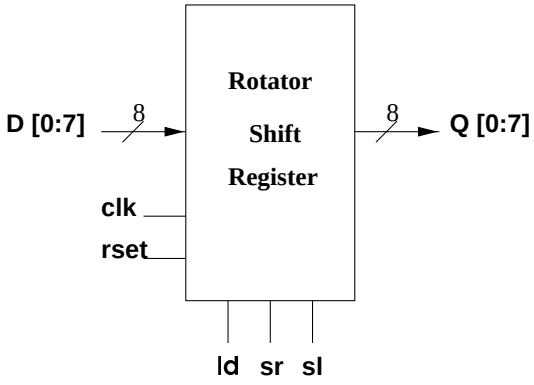
In the following figure the NMOS network of a complex CMOS logic gate is shown.

- **6.a)** Express the Boolean function of the gate.
- **6.b)** Draw the corresponding PMOS network inside the square.
- **6.c)** Size the transistors such that, in worst case, the logic gate has the same output resistance as an inverter with PMOS $W/L = 4$ and NMOS $W/L = 2$.



[7] HDL Design (10 marks, 20 minutes)

Write the full Verilog code for an eight bit circular shift register (i.e the carry out is fed back). It has an asynchronous Reset (rset), Clock (clk), Load (ld, for loading the register with data in a parallel fashion), shift left (sl), and shift right (sr) signals. You must use the given names in the figure.



Extra sheet